9865A
CASSETTE MEMORY
SERVICE MANUAL

HEWLETT hp PACKARD

9865A CASSETTE MEMORY

SERVICE MANUAL

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CHAPTER 1

GENERAL INFORMATION

INTRODUCTION

This manual will assist the -hp- Service Representative in servicing the 9865A Cassette Memory. Information in this manual includes installation, theory of operation, maintenance, pseudo-hardware, and troubleshooting.

GENERAL DESCRIPTION

The 9865A Cassette Memory is used with 9800 Series Calculators in applications where bulk data storage or lengthy program storage is required. Several cassette memories may be coupled to the calculator simultaneously, providing additional storage if required.

SERVICE CONCEPT

With the exception of the transport assembly, the cassette memory is serviced by component repair. The transport assembly is exchanged on the -hp- Blue Stripe Program. An initial set of cassette memory assemblies is provided in the 9865A Service Kit (11269A). A complete list of the service kit assemblies is provided at the back of this manual.

> NOTE
>
> In January of 1975, the 11269A Kit was changed to 11269B. The B kit is the same as the A kit except the 11256-69521 plug-in ROM has been deleted.

CHAPTER 2
INSTALLATION

POWER REQUIREMENTS

A line voltage selector card (located in the power module on the 9865A rear panel) enables the cassette memory to be operated on a line voltage of either 100, 120, 220, or 240 V ac (+5%, -10%). The line frequency must be within 48 to 440 Hz. The cassette memory requires a maximum of 50 voltamps.

GROUNDING REQUIREMENTS

To protect operating personnel, the cassette memory is equipped with a three-conductor power cable which grounds the cabinet of the cassette memory when connected to an appropriate power receptacle.

SETTING THE VOLTAGE SELECTOR CARD

The voltage selector card can be installed by performing the following procedure(refer to Figure 2-1):

1. Slide the clear plastic window on the power module all the way to the left.
2. Pull the FUSE PULL lever out to release the fuse; remove the fuse.
3. If the selector card is installed, it may be removed by using a sharp-pointed object (e.g., a ball point pen) to pry the card out of the module.
4. Install the card into the power module. The proper voltage selection is made when the number for the selected voltage is visible after the card is installed.
5. Return the FUSE PULL lever to its original position.
6. Install the appropriate fuse (see Table 2-1) into the fuse clip and slide the plastic window to the right.

Table 2-1. Line Voltage/ Fuse Selection

Nominal Voltage	Selector Card Position	Fuse	-hp- Part No.
90 - 105	100	.5A SB	2110-0202
108 - 126	120	.5A SB	2110-0202
198 - 231	220	.25A SB	2110-0201
216 - 252	240	.25A SB	2110-0201

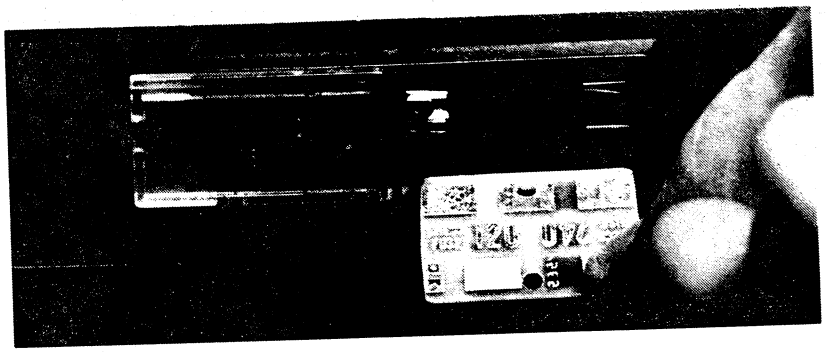


Figure 2-1. Setting the Voltage Selector Card

NOTE

9865A units with serial numbers 1205A 00250 and below have a different power module. Refer to the description below when setting the line voltage on these units.

SETTING THE LINE VOLTAGE SWITCH

The line voltage switch for 120V or 240V operation can be moved only when the fuse is taken out of the power module. With the fuse removed from the power module, and the FUSE PULL lever moved all the way to the left, use a narrow blunt instrument to slide the lever of the line voltage switch to the proper position. Be sure to move the lever of the switch as far as it will go, otherwise, the FUSE PULL lever cannot be returned to its normal position.

CHAPTER 2

INSTALLATION

100 AND 220V OPERATION

When shipped from the factory, the 9865A will operate on either 120V or 240V power lines (+5%/-10%). The 9865A can be rewired to operate on either 100V or 220V power lines (+5%/-10%). This is done by removing the grey wire from the power module and connecting it to the black/white wire which is lying loose in the wiring of the power transformer. Once these two wires are connected, the 120 switch position on the power module will select 100V operation; the 240 position will select 220V operation.

CAUTION

THIS MODIFICATION SHOULD ONLY BE MADE TO ALLOW THE CUSTOMER'S INSTRUMENT TO FUNCTION ON HIS NORMAL LINE VOLTAGE, NOT TO SATISFY A SEASONAL LOW LINE CONDITION. IF THIS MODIFICATION IS MADE AND THE LINE VOLTAGE EXCEEDS +5% OF THE SELECTED VOLTAGE (100V or 220V) DAMAGE TO THE POWER TRANSFORMER MAY RESULT.

CASSETTE MEMORY SELECT CODE

Since all calculator peripheral devices are connected in a 'party line' fashon, each device must have a unique 'address' so that the calculator can specify which device should respond to each operation. The cassette memory's address (or select code) consists of a one-digit number and is determined by the circuitry on the interface card. Each cassette memory operation must include the correct select code, thereby instructing the proper interface card to respond to the operation while all other cards ignore it.

The cassette memory may be set to any one of nine select codes by following the procedure given below. (Refer to figure 2.)

1. Switch the calculator and the cassette memory OFF.
2. Disconnect the cassette memory interface card from the calculator. Remove the four screws located on the top of the card assembly; then, turn the card over and lift off the bottom cover.
3. Locate the two select code jumper wires (PJ1 and PJ2). Notice that each wire connects one set of holes on the interface card. The sets of holes are numbered 1 through 9 - each set corresponds to a specific select code number.
4. To change the select code, both wire jumpers must be unsoldered, inserted into the sets of holes which correspond to the desired select code, and resoldered.
5. After resoldering both wire jumpers, carefully examine the board to ensure that excessive solder is not touching any of the adjacent holes.
6. Assemble the interface card assembly, and replace the select code labels on the cassette memory mainframe and interface card with ones which indicate the new select code.

Verify the electrical performance of the cassette memory by running the 9865A Cassette Memory Exerciser.

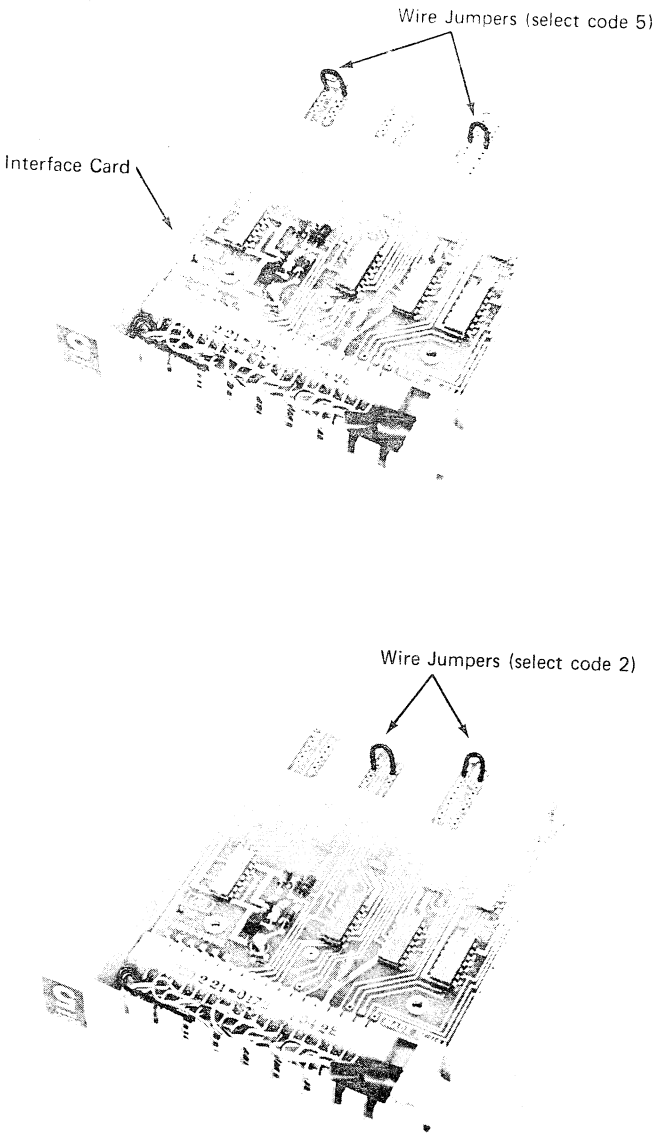


Figure 2 Changing the Select Code

CLEANING THE TAPE HEAD

As with most precision recording equipment, the cassette memory can be expected to provide trouble-free operation only if the user adheres to a scheme of regular preventative maintenance. The following tape-head cleaning procedure should be performed after every eight hours of cassette operation. Also, this procedure should be performed prior to making a 'permanent' cassette memory recording.

CAUTION

READ ALL OF THE FOLLOWING PROCEDURE AND INFORMATION SUPPLIED WITH THE TAPE HEAD CLEANER BEFORE PERFORMING THE CLEANING PROCEDURE.

To clean the tape head:

1. Rewind and remove the tape cassette, then switch the cassette memory OFF.
2. Remove any dust or other material that has accumulated in the vicinity of the tape head.
3. The tape head should be cleaned with a cotton applicator which has been dampened with head cleaning solution or denatured alcohol. It is sufficient to gently wipe the top of the head a few times, and then repeat wiping of the head with a clean applicator.

CAUTION

DO NOT ALLOW THE CLEANING SOLUTION TO TOUCH THE TAPE-TRANSPORT DOOR OR THE LIGHT-SENSING ASSEMBLY

4. Close the tape-transport door after cleaning the tape head. A good practice is to close the door whenever the cassette memory is not in use.

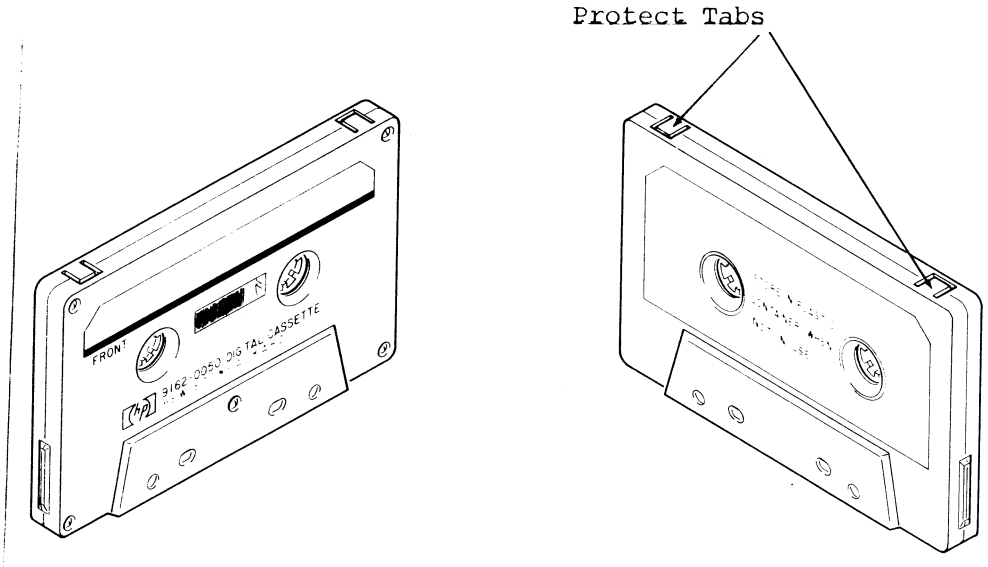


Figure 4. The Tape Cassette

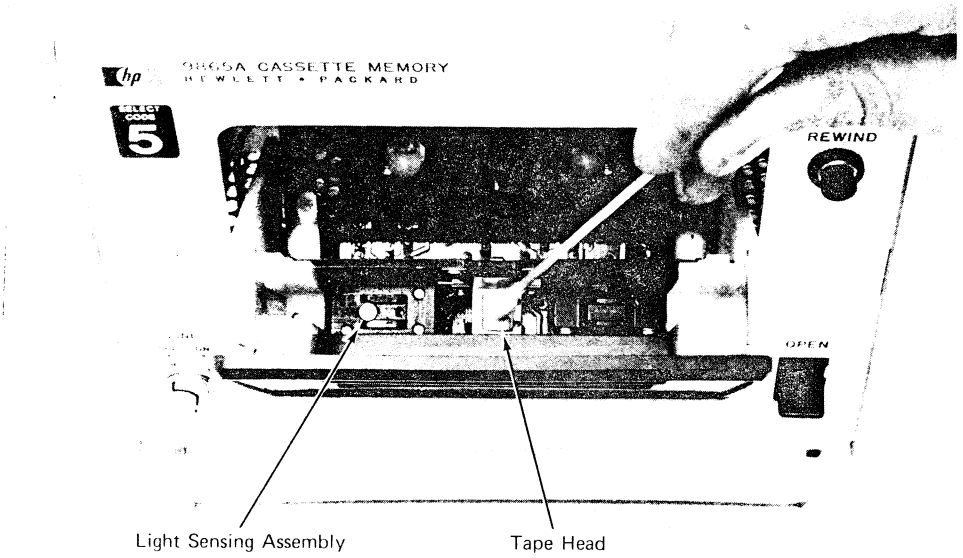


Figure 3 Cleaning the Tape Head

CHANGING THE FRONT PANEL LAMP

The LINE switch on the front panel of the cassette memory contains a neon light bulb. If the cassette memory functions normally, but the LINE switch fails to light, the bulb is probably defective. To change the bulb, switch the cassette memory OFF and pull the switch lens straight out; the bulb will come out with the lens. Remove the old bulb and place a new one, -hp- Part No. 2140-0244, into the lens. Now reinstall the lens.

THE TAPE CASSETTE

The tape cassette recommended for use in the cassette memory is shown in Figure 4. This cassette is a precision unit and contains three-hundred feet of digital-quality, magnetic recording tape. These and other important characteristics make this tape cassette ideally suited for use in the cassette memory.

The -hp- cassette is available in single quantities and in multiple quantities at a reduced price. When ordering the tape cassette, specify -hp- Part No. 9162-0050. (Available through CSC only.)

Although other available tape cassettes will initially work in the cassette memory, many of these products will not provide reliable cassette memory recordings. Also, since the use of colored tape cassettes (any color other than white) will actually damage the cassette memory Transport Assembly, -hp- cannot ensure cassette memory operation if it is used with a tape cassette not indicated above. Furthermore, -hp- will not warranty any damage to a cassette memory that is caused by the use of tape cassettes other than the one recommended.

NOTE

Since a vast amount of information can be stored on a single tape cassette, loss of the cassette's contents (e.g., normal tape wear, physical damage, exposure to a strong magnetic field, or instrument failure) could be extremely expensive to the user . . . both in time and resources lost. One method of preventing such a loss is to make a duplicate recording of each often-used or valuable tape, and then storing these 'master tapes' in a safe place. The practice of making master tapes (or making master recordings on magnetic cards) should be considered manditory when the application requires that the tape be used on a daily basis.

THE TAPE CASSETTE

The Protect Tabs

The information recorded on a tape cassette can be protected from loss due to subsequent recording operations by removing both protect tabs on top of the cassette (see Figure 4). The cassette memory will terminate any record operation on a cassette which has the protect tabs removed.

Storing Tape Cassettes

Each tape cassette is supplied with a plastic case, which should be used when storing the cassette, as the magnetic tape is delicate and can be easily damaged. Also, the tape should be fully rewound before it is removed from the cassette memory.

As with most magnetic tape products, the information stored in the tape cassette can be altered or destroyed by exposing the tape to a strong magnetic field, such as is produced by a bulk tape eraser, a toy magnet, or some metal-detection devices (e.g., equipment used at many airports). In some cases, the use of a steel container, such as an index box, will protect the tapes from magnetic fields.

INTRODUCTION

The 9865A has several normal, but unusual, operating characteristics that might cause a user to suspect the cassette memory or calculator of being defective. This section describes the 9865A pseudo-hardware problems. It is assumed, however, that the Field Service Engineer is familiar with normal cassette memory operation and an -hp- tape cassette is being used.

UNPREDICTABLE 'FIND FILE' OPERATIONS

The FIND FILE operation is dependant upon the operator knowing the current file number, total number of files that are marked on the tape, and the use of a properly marked tape. User errors may cause the cassette memory to search for non-existing files or to simply run fast-foward to the ending clear-leader.

UNUSUAL REWIND OPERATION

The following rules apply to the use of the 9865A REWIND button:

1.) The REWIND button must be held in until the completion of the preceding operation.
2.) The REWIND operation is terminated by any other (operation) instruction from the calculator.
3.) The REWIND operation is terminated if calculator power is lost.

9865A WILL NOT LOAD PROGRAMS

The 9865A will not load a program :

a. That is not terminated with an END statement.
b. That is larger than the file into which it is to be loaded.
c. That is a SECURED program in the calculator memory.

9810A SECURED AND PROTECTED PROGRAMS

FMT 5 (n) 1/x causes the 9865A to record and secure the program in the calculator memory. Once this is done, the program cannot be listed.

Care must be taken not to inadvertently press the 1/x key

9810A SECURED AND PROTECTED PROGRAMS (cont'd)

in place of the x^2 key which are adjacent to each other. Both keys cause the program in the calculator memory to be recorded on the magnetic tape, but the 1/x key secures the program.

Both protect tabs must be removed; when only one tab is removed, the program will be lost if the cassette is turned around and data or programs are recorded on the tape.

STATUS LIGHT(9810A)

The status light is lit when any operation is terminated by pressing the STOP key.

9865A WILL NOT 'MARK TAPE' (9810A)

The 9865A will not mark a tape if a Ø is in the x or y registers, or if the number in x or y is greater than 9999. The cassette memory will not write on a protected cassette.

NO CALCULATOR CONTROL

If the STOP key does not return calculator control, power to the 9865A may have been lost during some 9865A operation other than FIND FILE. To return calculator control:

1.) Switch the 9865A power OFF.
2.) Open the cassette memory door.
3.) Switch the power back ON.
4.) Press STOP; the calculator display should return.
5.) Close the cassette memory door.

OPERATIONS WITH THE 11264A PLUG-IN ROM

Unusual operations may occur if the 11264A Peripheral Control Rom is installed and FMT 4 is pressed instead of FMT 5. The operator must be careful to avoid this situation. These operations may be terminated by pressing FMT 5 (n) $\sqrt{x}$ or FMT 5 (n) CHG SIGN.

TYPE 11 FILE (9810A)

If a FIND FILE operation is performed and a file type 11 is displayed in the Z register of the calculator, the file is a secured file.

INCORRECT TAPE POSITIONING AFTER A 'MARK TAPE' OPERATION

It is possible for the tape to be improperly positioned after remarking a proviously marked tape. This occurs because of a file head in the slack tape area following the last file just marked. The Cassette Memory reads the old file head and understands it to be the file head of the last file just marked; i.e., the cassette memory assumes that it has already back spaced to the beginning of the last file marked.

This problem may be avoided by following the MARK TAPE operation with a BACKSPACE and a FIND FILE operation to ensure that the tape is correctly positioned. In addition, the user must not use the last file (extra file) that was marked.

Table 5-1. Mnemonic List for the Cassette Memory

AGD	Analog Ground
ARA	Analog Read A
ARB	Analog Read B
BFD	Blank Film Detect
CEO	Calculator Ready
CGD	Chassis Ground
CIN	Cassette In Place
CFI	Calculator Flag Input
CNT	Control (I/O Card to 9865A)
CO (Ø-3)	Select Code (from Calculator)
DI (Ø-7)	Data Input (to Calculator)
DO (Ø-7)	Data Output (from Calculator)
FLG	Flag (9865A to I/O)
FTC	Fast Command
ID (Ø-7)	Input Data (9865A to I/O)
INT	Interrupt
IS (Ø-3)	Input Status (9865A to I/O)
LDR	Clear Leader
LGD	Logic Ground
MCM	Motor Common
MCT	Motor Control
MFR	Motor Forward
MGD	Motor Ground
MLS	Mini-Loudspeaker Signal
MRV	Motor Reverse
OD (Ø-7)	Output Data (I/O to 9865A)
OS (Ø-3)	Output Status (I/O to 9865A)
POP	Power ON Preset
RCL	Read Clock
RDT	Read Data
RMK	Read Mark
RNC	Run Command
RVC	Reverse Command
RWD	Rewind
SCD	Select Code
SI (Ø-3)	Status Input (I/O to Calculator)
SIH	Service Interrupt Inhibit
SO (Ø-3)	Status Output (Calculator to I/O)
SFR	Solenoid Forward
SRV	Solenoid Reverse
SSI	Service Interrupt Request (to Calculator)
STP	STOP (internal in 9865A logic)
THA	Threshold A
THB	Threshold B
WCL	Write Clock
WDA	Write Data A
WDB	Write Data B
WDT	Write Data
WEN	Write Enable
WMK	Write Mark
WPT	Write Permit (From light sensors when protect tabs are removed.)
WTC	Write Command

INTRODUCTION

This section provides the principles of the operation of the cassette memory. It is presumed that the reader is thoroughly familiar with normal cassette memory operation, and has had some experience with calculator and cassette memory operations.

Logic Definitions

Except where otherwise noted, the following logic conventions are used when describing cassette memory signals:

A. Logic levels are nominally Ø volts and +5 volts; ØV is referred to as the 'low' state and +5V is referred to as the 'high' state.

B. Logic signals are given three-character mnemonics as listed in Table 1. The mnemonics are of two types:

1) Those preceded by the letter 'N' (not); these signals are low when true and may be seen on the schematics as a three-character mnemonic with a bar over all three characters; i.e., NFTC = $\overline{\text{FTC}}$ = a low true fast tape command.

2) Those signals preceded by the letter 'Y' (yes); these signals are high when true and may be shown on the schematics as a three-character mnemonic. For example, a high LEADER signal would be either YLDR or LDR.

GENERAL DESCRIPTION

The cassette memory adds to the basic memory storage capability of a 9800 Series Calculator. Control of the cassette memory is accomplished from the calculator through an appropriate plug-in ROM Block such as the 11265A (Model 10) or 11224A (Model 20). Instructions to the cassette memory are presented at the External I/O slots in the form of ASCII-coded data signals. The 9821A and 9830A calculators do not require a plug-in ROM for cassette operation.

The I/O Card plugs into any of the calculator I/O slots. The function of the I/O Card is to provide the cassette memory select code and to coordinate and buffer the data exchange between the cassette memory and the calculator. When the sending device has data to be transferred, the I/O accepts the data, performs any necessary buffering and logic operations, and outputs the data when the receiving device is ready. Power for the I/O Card is provided by +5V from the calculator. A +5V dc reference from the cassette memory is used in the 'Power Up' sense circuit.

The Control Logic Board (A2) decodes the ASCII and STATUS outputs from the I/O Card when the cassette memory is receiving data from the calculator and compiles the ASCII data when the cassette memory is sending data to the calculator. The Control Logic Board determines the sequence of events which occurs in either a read or write operation. The control logic also responds to transport and system status conditions and translates the (read/write) data signals going to and from the Read/Write Board (A3).

The Read/Write (R/W) Board has two major functions:

A. In the write mode, it encodes bit serial data into two-channel Bit-Mark-Sequence (BMS) data to be stored on the magnetic tape.

B. In the read mode, it decodes the two-channel, analog, BMS data from the tape into clock, mark, and bit-serial pulses.

The Motor Control Board (A4) determines and monitors the speed of the tape-drive motors. Outputs of the Motor Control Board provide high and low-speed bidirectional tape movement through two drive motors that are located in the transport assembly.

The filter and Regulator Boards (A7 and A8) provide +17Vdc, ±12Vdc, and +5Vdc power to the cassette memory. All grounds are terminated at one 'node' on the Regulator Board to minimize ground currents.

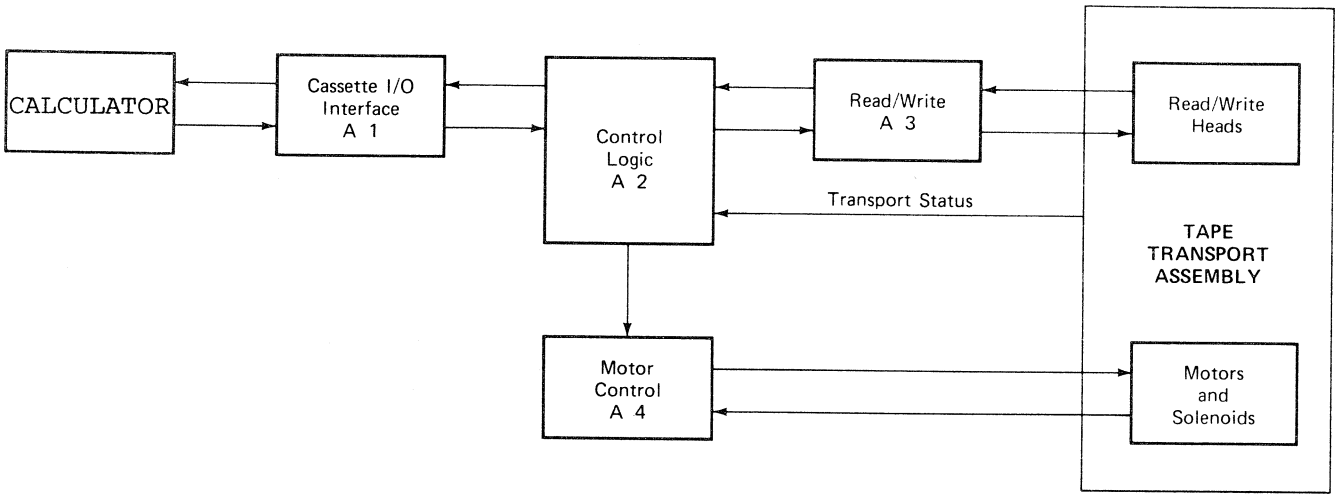


Figure 5 Cassette Memory Block Diagram

CASSETTE MEMORY I/O CARD (A1)

See Figure A1

Power Up

The I/O Card 'Power Up' sense circuit consists of the four transistors, Q1 through Q4, and their associated components. All four transistors are normally not conducting. Q1 or Q2 is switched on if the cassette memory and the calculator +5V supplies differ by more than 1.5V. If Q1 or Q2 is switched on, Q3 and Q4 are switched on, and output a logical Ø. The output of Q3 is seen by the control logic as a LOW INTERRUPT signal. The output of Q4 forces the 10/20 line to a logical Ø and disables the I/O interrupt logic circuits. The 10/20 data line and interrupt logic circuits are discussed later in this section.

Cassette Memory Operations

Each cassette memory operation begins by the calculator checking the cassette memory status. This is accomplished by the calculator addressing the peripheral and holding the CALCULATOR READY (NCEO) signal high. The peripheral address (select code) is decoded by U1, and, if PJ1 and the select code are in agreement, U8a is enabled; thus U2 is enabled and outputs cassette memory status to the calculator.

If the calculator finds the status conditions satisfactory for further operations (the leader status bit, SI2, is ignored) the CALCULATOR READY (NCEO) is forced high disabling U8a and enabling U8b. U8b enables U3 and U4. In this condition, the I/O card is set for mutual data exchange between the calculator and the cassette memory.

When U8b is enabled, its output is twice inverted and seen by the Control Logic Assembly (A2) as a control (YCNT) signal which causes the control logic to begin processing the calculator output data.

The U8b output is also the D input to U12a, and when the signal FLAG (YFLG) is received from the control logic U12a is clocked and U7b is enabled. U7b, when enabled, outputs the signal CALCULATOR FLAG INPUT (NCFI), which informs the calculator that the cassette memory has begun processing the calculator output data and has data for the calculator on the I/O card output lines (DIØ-DI7)

CASSETTE MEMORY I/O CARD (A1)

Cassette Memory Operations (cont'd)

If the cassette memory is performing an operation (correct select code and NCEO low) and the cassette door is opened, U12a is preset causing U7b to output the signal CALCULATOR FLAG INPUT (NCFI). The calculator then checks the cassette memory status (as previously described) and the operation is aborted.

Interrupt Operation

When used with the MODEL 20 calculator the cassette memory can request calculator service if U13c is enabled by any one of the following conditions occurring:

A. If the cassette door is opened.

B. If the cassette runs onto the clear leader.

C. If the cassette memory reads an interrupting character on the tape. (The only interrupting character is the beginning-of-file mark, which is described in the READ/WRITE assembly Theory of Operation).

The U13c output clocks U12b, and, if the D input of U12b is high, U7a and U7d are partially enabled. The D input of U12b is high if U8b is disabled, the cassette memory is in the CONTROL MODE (ISØ high), and the 10/20 data line is high (MODEL 20 operation).

U7a and U7d are enabled by U12b if the signal SERVICE INTERRUPT INHIBIT (NSIH) is high, and output the peripheral SELECT CODE (NSCD) and SERVICE INTERRUPT REQUEST (NSSI) to the calculator.

NOTE

The select code output of U7d passes through PJ2. Therefore, PJ2 and PJ1 must be set to the same select code before the calculator will recognize the cassette memory as the interrupting peripheral.

CONTROL LOGIC ASSEMBLY (A2)

Refer to
Figure A2-1 A2-2

Power ON Preset

A 'POP' circuit is included on the Control Logic Board to ensure that the cassette memory powers up in the proper mode. The 'POP' circuit consists of Q1, CR2, and C1.

When the cassette memory is initially switched ON, +5V is applied to the input of inverter U2 and C1 begins charging to +5V through R1. A charge on C1 of approximately 2.7V causes the Zener diode CR2 to break down. CR2 conducting through R3 switches Q1 on. Q1 conducting through R2 forces the input of U2 to a logical Ø.

The initial high U2 input is inverted to make a NPOP pulse. This pulse ensures that U10c is disabled. The low U10c output clears the data latch (U20), disables U1b and U16d, and clears flip-flops U15a and b.

When Q1 is switched on, the NPOP pulse is removed from the logic circuits and the control logic is ready to begin processing data from the I/O Card.

Status Data Processing

	INPUTS		
	FAST	REVERSE	WRITE
Operation	OSØ	OS1	OS2
Forward	low	low	low
Fast Forward	high	low	low
Reverse	low	high	low
Fast Reverse	high	high	low
Write	low	low	high

The status data outputs of the I/O Card appear on data lines OSØ - OS3 as control logic command inputs. These commands are used as inputs to U10 (a one-of-ten bit decoder) and U20 (a data latch).

Data lines OSØ - OS2 input data to U10. A fourth input to U10 comes from the control one-shot (U7) $\bar{Q}$ output. U7 has a 300nS output when triggered by the positive edge of the control (YCNT) input from the I/O Card.

CONTROL LOGIC ASSEMBLY (A2)

Status Data Processing (cont'd)

When the calculator STOP key is pressed, the decoder's B and D inputs go low and the A and C inputs go high, causing the pin 6 output to go low. This low is the signal STOP (NSTP) that disables U10c, presetting the control logic as described in the 'POP' section.

The 300nS Q output of U7 partially enables U16a. U16a is fully enabled if the latch, U20, shows the cassette memory to be in the write mode (pin 12 high). The U16a output is the LOAD signal for the 9-bit shift register, which causes the shift register to store the data from the I/O assembly.

The output of the decoder cannot be low unless the D input is low. The D input is low only when U7 has a 300nS output, at which time the inputs are decoded and one low input forces the output(s) low. The low decoder output clocks the data latch (U20), presets the Run flip-flop, and the trailing edge of the decoder output clocks the Rewind Flip-flop.

When the clock input of U20 is low, the outputs of the data latch follow the inputs. The data is latched at the trailing edge of the 300nS decoder output.

The low preset input to the Run flip-flop forces the Q output high, thereby enabling U17c (which enables the motor drive circuits on the Motor Control Board), and partially enabling U16b. The Q output is also the signal RUN ENABLE for the Divide-by-ten logic circuits which are described later in this section.

A high signal on data line OS2 (when latched by U20) fully enables U16b. The high U16b output is seen by the R/W Memory Board as a WRITE COMMAND (YWTC) signal. The WRITE COMMAND (YWTC) signal also goes to U2, U14, U8a, U8b, U17d and the 3 KHz Clock. Each of these logic operations are described in the Control Logic ASCII Translation section of this chapter.

U15a is the Rewind flip-flop and is preset by a (low) REWIND (NRWD) signal when the REWIND button is pressed. If the cassette memory is not performing a calculator command, U15b is cleared, enabling U16c, and a RUN-FAST-REVERSE command is initiated to the Motor Control Board. The rewind operation is terminated by either the tape

CONTROL LOGIC ASSEMBLY (A2)

Status Data Processing (cont'd)

onto the clear leader (which clears U15a) or a new calculator command presetting U15b.

Control Logic Operation Commands

The outputs of the data latch (U20) enables the proper gate U17a, b, and c. (The U16b was described in the Status Data Processing section.) The combined outputs of these three gates and U16b, determine the operation which the cassette memory is performing. See Table 2.

TABLE 2.

OUTPUTS

Operation	U17A FTC	U17B RVC	U17C WTC	U16B RNC
Forward	1	1	0	0
Fast Forward	0	1	0	0
Reverse	1	0	0	0
Fast Reverse	0	0	1	0
Write	1	1	1	0

The Operation Command outputs are seen by the R/W Board or Motor Control Board as commands to perform the operation(s) indicated by the combination of all four commands. The outputs are also used in other control logic operations, and frequent reference to them is made throughout the remainder of the Control Logic Assembly description.

Status Outputs

The control logic outputs four status signals to the I/O Card. These outputs are:

IS$\emptyset$ . . . . . Mode (high = control; low = data mode)
IS1 . . . . . WRITE PERMIT (NWPT)
IS2 . . . . . CLEAR LEADER (YLDR)
IS3 . . . . . CASSETTE IN (NCIN)

CONTROL LOGIC ASSEMBLY (A2)

Status Outputs (cont'd)

Each calculator command contains a (Control - Data) MODE signal on data line SO3. The I/O Card outputs this signal to the control logic (OS3) where is is latched by U20. The output of U20 pin 10 is buffered by U10a and serves as one input to U4. The U10a output appears on data line ISØ, and is one input to U18a. U18a and U4 are described later in this section.

The signal WRITE PERMIT (YWPT) comes from the tape transport assembly, and is high if the tape cassette is not protected. The WRITE PERMIT signal is inverted and appears as a NWPT signal on data line IS1.

The control logic monitors and outputs the two tape transport status signals LEADER (YLDR) and CASSETTE IN (NCIN).

The LEADER (YLDR) signal enables U1a. (U1a is a Schmitt-trigger input gate, and serves as a filter on the LEADER [YLDR] input line to prevent line noise interferrence with cassette memory operations.) The U1a output is inverted and clocks the RUN flip-flop which disables U17c. The U1a output is also inverted and appears on data line IS2.

U1b is partially enabled by the CASSETTE IN (NCIN) signal, which is an output on the IS3 data line. A high U10c output, and a high INTERRUPT (NINT) signal from the I/O Card fully enables U1b. The low U1b output enables U9c and U9c partially enables U16d. U16d is full7 enabled by a high LEADER (NLDR) input signal. The U16d output is the clear input to U15a. Both U15a and b require a low clear input, and if an input to U1b is low, or if the LEADER (NLDR) signal is low, the two flip-flop outputs disable U16c and U17c to abort the operation. The cassette must be in before any further operations can be performed. However, the tape can be moved off of clear leader to perform new operations whenever necessary.

ASCII Data Translation

U3, U4, U5b, U12a, and U12b comprise a nine-bit shift register. During write operations, the shift register is loaded parallel by the LOAD signal from U16a. The ASCII data is then translated and shifted to U3 pin 10 to be written on the tape. During a read operation, the data from the R/W Board is clocked (by a clock signal from the tape) serially from the D input of U5b into the shift register and

CONTROL LOGIC ASSEMBLY (A2)

ASCII Data Translation (cont'd)

loaded parallel onto the output lines. When U9b outputs a **FLAG** signal, the I/O inputs the parallel data.

During write operations, WRITE CLOCK (YWCL), WRITE DATA (YWDT), and WRITE MARK (YWMK) signals are control logic outputs to the R/W Board. During read operations, the signals are inputs to the control logic from the R/W board as READ CLOCK (NRCL), READ DATA (YRDT), and READ MARK (YRMK) signals. When the 'read' signals are properly sequenced, they constitute a character. The sequence of data is 9 data bits per character; each character separated by a mark. (This sequence, called a Bit Mark Sequence, is described, in detail, in the READ/WRITE Assembly Theory of Operation.)

The center bit of the 9-bit character is called a CONTROL bit. If the center bit is a logical 1 the character is a control character, and a logical Ø constitutes a data character.

3 KHz Write Clock

One-shots U6 and U13 make up an asymmetrical 3 KHz clock. U6 has a high output for 133uS and a low output for 200uS (R9 is padded by R10 to give a 3 KHz rate at TP1).

The trailing edge of the U6 Q output clocks U13. A high U6 Q output partially enables U18d and U10b. The U6 $\bar{Q}$ output enables U12d, and the U12d output clocks the divide-by-ten counter U14. U14 is also clocked through U12 by a low NRCL signal.

The clock is enabled by the WRITE COMMAND (YWTC) signal (from U16B) on U13 pin 5. The end of the YWTC signal inhibits the clock.

Divide-by-ten Counter (U14)

The Divide-by-ten logic circuits determine the sequence that data is written on the magnetic tape. This data must then be read by the cassette memory in that sequence before it will be recognized by the decode counter as legitimate characters.

CONTROL LOGIC ASSEMBLY (A2)

Divide-by-ten Counter (U14) (cont'd)

The decade counter outputs a high signal to enable U18c one of every ten 3 KHz clock outputs. (High inputs on pin 2 and 3 force the counter to Ø; high inputs on pins 6 and 7 force the counter to 9.) The output of U18c is high nine counts (0-8) for every 10 clock outputs. The U18c output enables U18d (when the clock is high) for 9 of 10 counts; the low output (9) is inverted to fully enable U10b at a count of 9, when the clock output (TP1) is high.

The output of U18d (enabled 9 of 10 clock outputs) is inverted and seen by the R/W board as a WRITE CLOCK (YWCL) signal. The low output of U18d or a low READ CLOCK (NRCL) signal from the R/W board enables U18b. U18b partially enables U10d. U10d is fully enabled by the RUN ENABLE signal from the Run flip-flop. The output of U10d causes the 9-bit shift register to right-shift during read or write operations.

The output of U10b is high one of ten (9) clock outputs. The U10b output is seen by the R/W board as a WRITE MARK (YWMK) signal, partially enables U12c, and is inverted to clear U8b.

U12c is fully enabled by the high $\bar{Q}$ output of U8a. The U8a output is low when WRITE COMMAND (YWTC) clocks the flip-flop, thus disabling U12c until the counter reaches the first count. At the first count of 9, U18d clears U8a forcing the $\bar{Q}$ output high. The high U8a output together with a high U10b output enables U9b and generates a FLAG each time a character is written.

Flag

The previous discussion described how a FLAG is generated during write operations. U9a, when enabled, enables U9b to output a FLAG during Read operations. This occurs when a character is read in the data Mode, or when a control character is read in the control Mode. (A control character has been read when pin 5 of U11 is high.)

A STOP signal (from the ROM) also enables the Flag gate U9b, which outputs a FLAG to the I/O Card.

CONTROL LOGIC ASSEMBLY (A2)

Counter Presetting

U8b, together with a high WRITE COMMAND (YWTC) signal, forces the counter to 9 when the signal WTC first goes high. This forces the first bit written to be a MARK. (U8a prevents a FLAG from being generated at this MARK.) U8b is cleared as soon as this first mark is written.

U5a, together with a high WRITE COMMAND (NWTC) signal, forces the counter to Ø when the logic is in the Read mode and U5a is either preset by a false RUN ENABLE signal (no operations being performed) or clocked (by YRMK) when a Mark has been read.

READ/WRITE MEMORY ASSEMBLY (A3)

Refer to Figure A3 and Figure 6

General Description

The R/W Memory Board encodes bit-serial data into two-channel, Bit-Mark-Sequence (BMS) data during a Write operation, and decodes the two-channel BMS data (from the tape-head preamplifiers) into clock, mark, and bit-serial data during a Read operation.

During a Read operation, the R/W board must also detect the tape speed and shape the analog signal from the tape head into a digital signal of the same time duration.

Threshold Detector

The analog signals from the tape-head preamplifiers are proportional in amplitude to the tape speed. The Threshold Detector (U6a and U6b), together with the Tape-Speed Detector (Q1 and Q2), converts the tape-head analog signals into digital signals.

NOTE

The A- and B-channel Threshold Detectors function in the same manner; therefore, only the A-channel (ARA bit with U6a) is described here.

The signal YARA is the input data from the tape-head preamps to the + input of the operational amplifier (U6a). When the analog signal reaches a large enough voltage level, the U6a output switches from one saturated state to another. The U6a + input and output are of the same polarity; however, the output switches from one saturated state to the opposite state, thus outputting a ±10V square-wave for each ac input signal.

Assuming the YARA input to initially be positive-going, the positive output of U6a is coupled by R14 to the bases of Q3 and Q4. Q3, then, switches on, clamping its collector to ground (along with any signal from Q1). Q4 switches off, and the U6a-input senses the voltage present between R8 and R9.

READ/WRITE MEMORY ASSEMBLY (A3)

Threshold Detector (cont'd)

NOTE

The voltage levels between R4-R5 and R8-R9 are dependent upon tape speed and are described in the Tape-Speed Detector section of this description.

The negative voltage now present on the - input of U6a determines how far negative the YARA signal must go before U6a switches to the negative output state. When the YARA signal is of a sufficient negative value, U6a switches states, turning Q3 off and Q4 on. The voltage (from Q2) on the collector of Q4 is now clamped to ground and the positive voltage between R4 and R5 references U6a for the next positive input signal.

Threshold Detector Output Shaping

The U6a output is positive limited to approximately +5V by CR3. CR4 clamps the negative portion of the U6a output to ground. The output of CR3 and CR4 is the signal YTHA and is one input to U1a. (The signal YARB, squared by U6b and shaped by CR9 and CR10, is the signal YTHB and one input to U1b.)

Tape-Speed Detector

The signals YARA and YARB are proportional in amplitude to the tape speed. To prevent tape noise from switching the Threshold Detector, when operating at high speed, the Tape-Speed Detector outputs a greater dc voltage (proportional to tape speed) to decrease the sensitivity of U6a and U6b. The - input of U6a and U6b is, therefore, polarity switched by Q3 - Q6, and desensitized by Q1 and Q2 increasing the voltage level of the Q3 - Q6 polarity outputs.

A low NFTC (low = FAST TAPE COMMAND) signal switches Q1 and Q2 off. Both transistors being off allows current to flow through R6 and R7, thus causing an increase in both the positive voltage between R4 and R5 and the negative voltage between R8 and R9 (more negative). Depending upon the Q3-Q4 and Q5-Q6 switching states, the increase in voltage levels is sensed by the - input of U6a and U6b. (When Q3 and

READ/WRITE MEMORY ASSEMBLY (A3)

Tape-Speed Detector (cont'd)

Q4 switch states, the opposite polarity is sensed by U6a.) The increase in reference voltages increases the threshold of U6a and b, thus decreasing the sensitivity of the Threshold Detector.

When the NFTC signal is high, Q1 and Q2 are switched on, and R6 and R7 are clamped to ground. This decreases the voltage sensed by Q6a and b and increases the sensitivity of the Threshold Detector.

Read Logic

A low WRITE COMMAND (YWTC) signal enables U1a and U1b, thus enabling the Read logic circuits.

When a MARK is read, both threshold bits (YTHA and YTHB) are high enabling U3c, and U9a is cleared. The high $\bar{Q}$ output of U9a is the signal READ MARK (YRMK), and also disables U5b forcing the READ CLOCK (NRCL) high.

U5a is enabled when either threshold bit is high and the trailing edge of the U5b output triggers the .5µS one-shot (U8) each time a data bit is read. The U8 output clocks U9a and (with the, now, clocked U9a low $\bar{Q}$ output) enables U5b to generate the .5µS READ CLOCK (NRCL) signal. U9a continues to have a high Q and low $\bar{Q}$ output until the next time a mark is read.

When threshold bit B (YTHB) is high U9b is preset by U5c unless U9a is cleared by a mark. This forces the READ DATA (YRDT) signal low each time YTHB is low.

U9b is cleared each time the YTHA bit is high except when a mark is read, thus generating the signal READ DATA (YRDT) each high channel A bit except for a mark.

Write Logic

The write logic is enabled by both the WRITE PERMIT (YWPT) and WRITE COMMAND (YWTC) signals going high and enabling U1c. The output of U1c switches Q7 on, thus generating the WRITE ENABLE (YWEN) signal.

READ/WRITE MEMORY ASSEMBLY (A3)

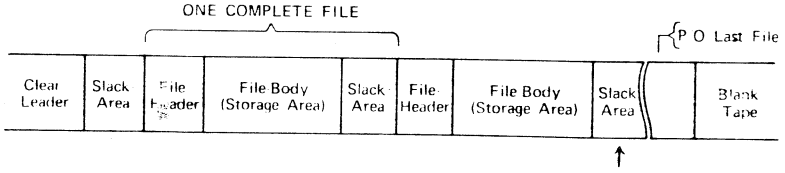
Write Logic (cont'd)

A high WRITE MARK (YWMK) signal enables U3a and U3b, and forces the signals WRITE DATA A and B (WDA and WDB) high for the duration of the WRITE CLOCK (YWCL) signal.

Data is written on the tape when the WRITE DATA (YWDT) signal goes high, forcing the YWDA signal high and the YWDB signal low for the duration of the WRITE CLOCK signal. A low WRITE DATA (YWDT) signal reverses the YWDA and YWDB output levels.

File Marking Format

The format shown below is used when each file is marked. Each file consists of a file-header, a file-body, and a length of slack tape. The length of each file is determined by the file-size specification (Y-register contents).



The File Marking Format

The file-header contains information such as the Beginning of file mark, the file number, type (data, program, or unused), absolute size, and current size (number of registers currently in use). The file-body contains space for storing a specified number of data (registers). The slack-tape, which is at the end of each file, provides an area within which the tape stops after each cassette control operation (see arrow in Figure). When the tape is stopped within the slack-tape area of one file, the cassette memory is ready to record into, load from, or identify, the next file on the tape.

The 'Beginning of File mark'(BOF) is the only CONTROL, or INTERRUPTING, character that is marked on the magnetic tape. The BOF is written at the beginning of each File Header. The File Header is used to determine the location of the tape during 'FIND FILE' operations.

READ/WRITE MEMORY ASSEMBLY (A3)

File Marking Format (cont'd)

During the execution of each MODEL 10 'FIND FILE' operation, the calculator determines the current file number, the direction the tape must be moved to locate the specified file (forward or backward), and the number of files that must be spaced to position the tape at the specified file. The calculator counts each BOF as the tape is spaced toward the specified file and stops the tape after the correct number of BOF's has been read.

MODEL 20 'SEARCH' operations are similar, except that the cassette memory stops (although it may not be noticable) at each file header between the current and specified files.

Bit Mark Sequence

Every character that is written on the magnetic tape must be present in a predetermined sequence called a Bit Mark Sequence (BMS). This sequence is a marker bit followed by the nine bit character. The cassette memory does not recognize characters which are not read in this sequence.

Each nine bit character is composed of: four bits-a control bit-four bits. The control bit determines if the character is a control or data character (BOF is the only control character). Each bit of a character uses channels A and B of the magnetic tape as shown in the Table below.

	Channel	A	B
	logical Ø	Ø	1
WDT	logical 1	1	Ø
WMK	marker	1	1

The control bit is a logical 1 for a control character and a logical Ø for a data character.

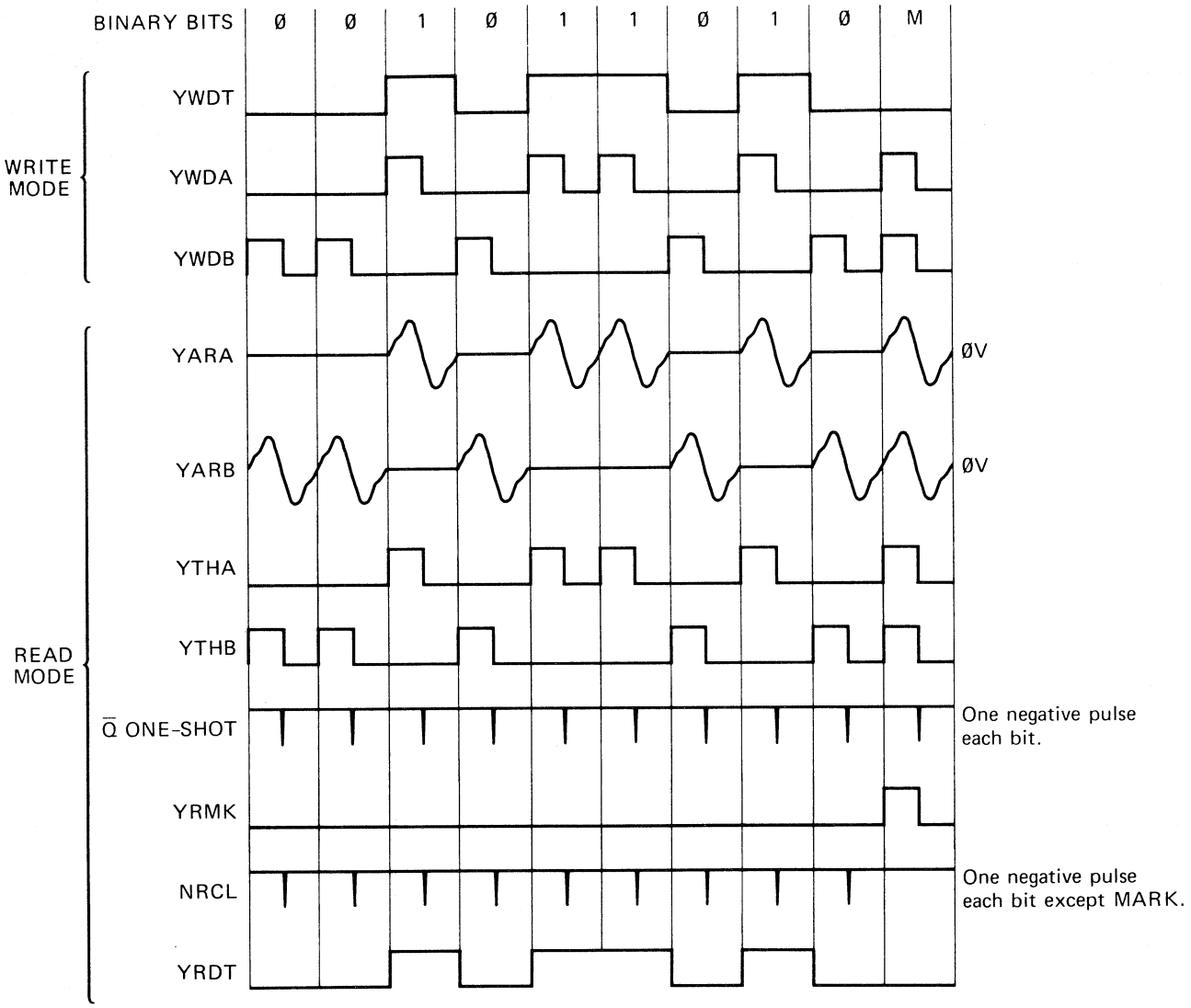


FIGURE 6

R/W BOARD WAVEFORMS

MOTOR CONTROL ASSEMBLY (A4)

Refer to Figures 7 and A4

General Description

The Motor Control Board controls the current (to the transport ass'y) that gives high-low motor speeds and energizes the foward-reverse solenoids. It also regulates the motor speeds, and drive-motor torque is reduced when the Tape Cassette is on the clear leader, thus preventing excessive wear of the transport's tape-drive mechanism.

Motor and Solenoid Drive Circuits

U2 enables either the foward (Q6, Q7, and Q9) or reverse (Q4, Q5, and Q8) driver circuits. Each circuit energizes the solenoid and drive motor that is the collector load for the output transistor.

Motor Drive voltage is applied through the drive motor to the drive transitors. As the motor turns, it generates a back-EMF voltage which is proportional to the speed of the drive motor

Motor-Speed Detector

The current used by the drive motor must pass through sensing resistor R9. R9, along with R10 - R14 input the motor terminal voltage and a voltage proportional to the total motor current. The signal at the output of U4 is proportional to the drive-motor speed. The U4 output goes to the motor-speed control circuits.

MOTOR CONTROL ASSEMBLY (A4)

Motor-speed Control

The inputs to U3 are the high-low speed command (NFTC) and motor speed. U3 outputs the difference of the inputs to Q2 through Q1. The (Q2) current through R7 changes the biase on the 'motor pass' transistor (on the Regulator Board) and regulates the current available to the drive motors, thus the speed of the motors.

When the tape cassette runs onto the clear leader, Q3 is switched on and reduces the current to the drive motor. The effect of this is to reduce the drive-motor torque to the tape cassette, and reduces wear on the friction-drive mechanism in the transport ass'y. A full torque condition cannot be regained until the end of the high YLDR signal.

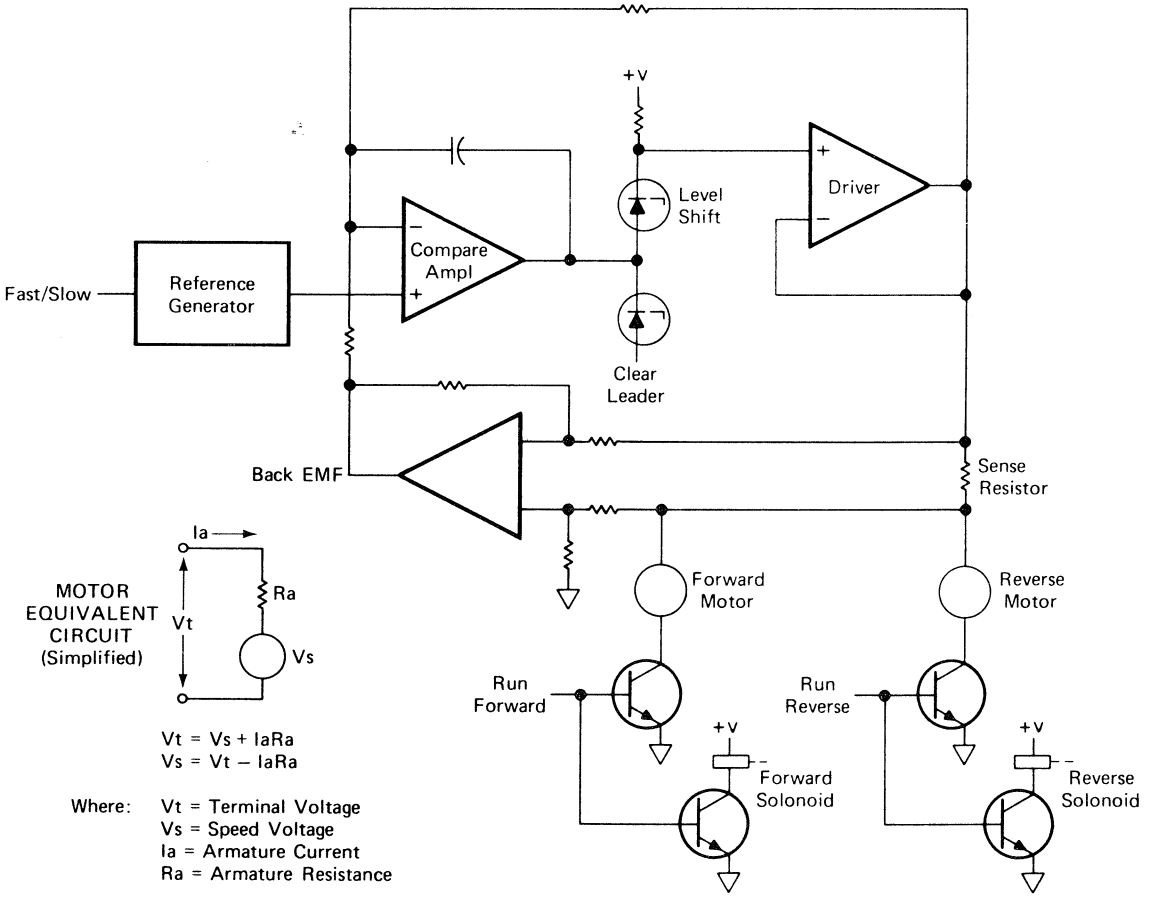


Figure 7 . Cassette Motor Control Assembly Block Diagram

POWER SUPPLIES (A7 and A8)

Refer to Figure A5
Rectifiers and Filters

Each of the three supplies (+12V, -12V, and +5V) employs a full-wave bridge rectifier and a filter capacitor. These components are located on the Filter Board (A7). All other power supply functions, described below, are performed on the Regulator Board (A8).

+5V Supply

The +5V supply is a self contained IC regulator with thermal foldback current limiting (about 1 amp) and thermal shutdown. The SCR (CR1) is activated only when the supply voltage exceeds 6 volts, and clamps the supply to a low voltage to prevent damage to 'downstream' devices.

-12V Supply

The -12V supply uses an IC regulator whose internal reference is compared to the supply output voltage thru R13 and R14. Resistor R12 senses the supply current to provide current limiting at about 120 mA. R10 ensures turnoff for pass transistor Q3.

+12V Supply

The +12V supply also uses an IC regulator. The internal reference is not used; instead, the + 12V supply is 'slaved' to the -12V supply by resistors R1, R2, R6, and R7. This provides +12V and -12V adjustment by simply selecting the value of R15 in the -12V supply. R5 current limits the supply at about 1 amp, and R3 ensures turnoff of the pass transistor Q2.

POWER SUPPLIES (A7 and A8)

Motor Pass Transistor (Q1)

The motor pass transistor (Q1) is located on the Regulator Board to provide proper heat sinking. This transistor operates on the unregulated +12V supply; connections from the base and emitter of Q1 go to the Motor Control Board (A4), where the pass transistor becomes part of the motor-drive circuitry.

Ground System

There are four distinct ground lines in the 9865A Cassette Memory. These are:

A. AGD - Analog Ground - low level analog ground.

B. LGD - Logic Ground - digital ground.

C. MGD - Motor Ground - grounds the motors and solenoids

D. CGD - Chassis Ground - 'third-wire' power line and shield ground.

These four grounds are brought together at a single 'node' on the Regulator Board to avoid unecessary ground currents.

The schematic designates the various grounds with the first letter (A, L, M, and C) of the three character mnemonic shown above. It is recommended that the ground shown with an individual circuit be used when troubleshooting that circuit.

INTRODUCTION

This section contains test procedures and troubleshooting hints that will assist the Field Service Engineer in the service and repair of a defective 9865A Cassette Memory. It is assumed, however, that the Field Service Engineer is familiar with normal Cassette Memory and calculator operation.

TEST EQUIPMENT RECOMMENDED

Below is a complete list of the test equipment that is recommended to efficiently service and repair a 9865A:

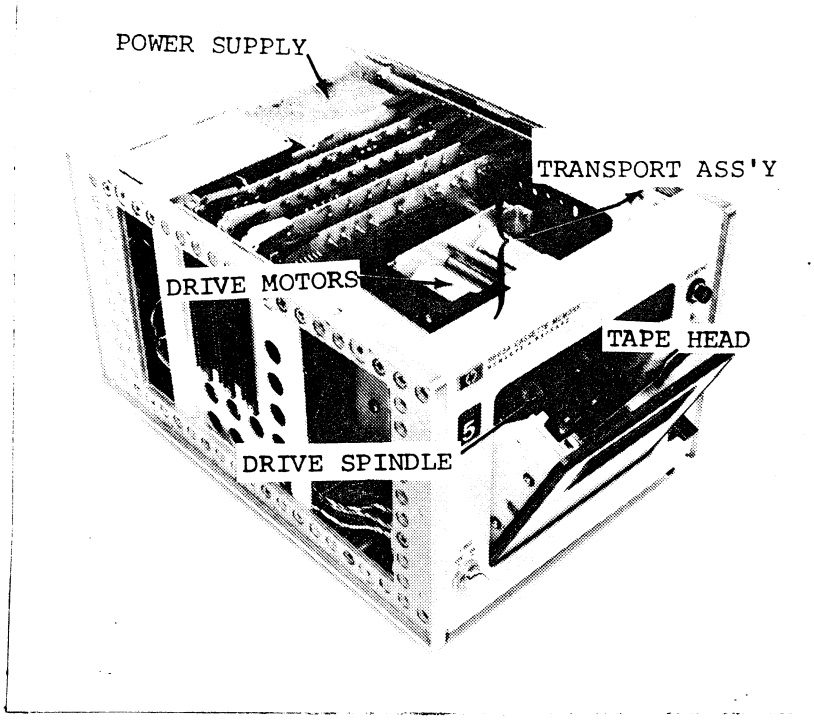
1.) POZIDRIVE phillips driver
2.) Solder iron and solder
3.) -hp- 427A
4.) -hp- 10525A Logic Probe
5.) 3-12" jumpers, with mini-alligator clips on each end.
6.) Premarked and protected tape cassette.

Two items which are sometimes useful are:

1.) -hp- 180A Oscilloscope
2.) -hp- 3440A or its equivelant

NOTE

Item number 6 (above) is not provided in the 11269A Service Kit. It is recommended that the Field Service Engineer mark a tape with at least 100 2-register files and remove the cassette protect tabs. This tape is useful in determining if the Cassette Memory will read information on a known good cassette. Should you wish to write on the tape after the protect tabs have been removed, simply cover the holes with cellophane tape.



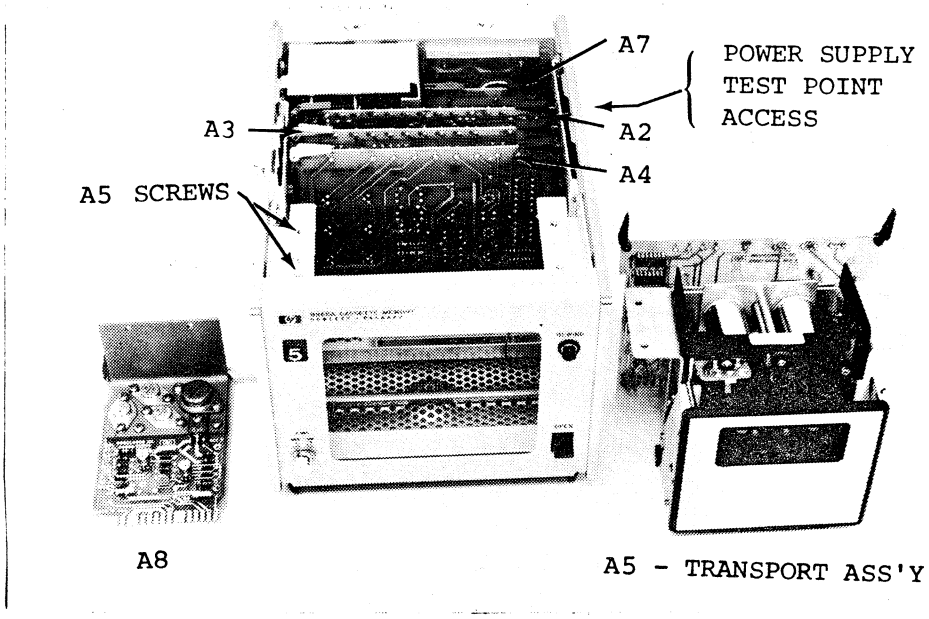
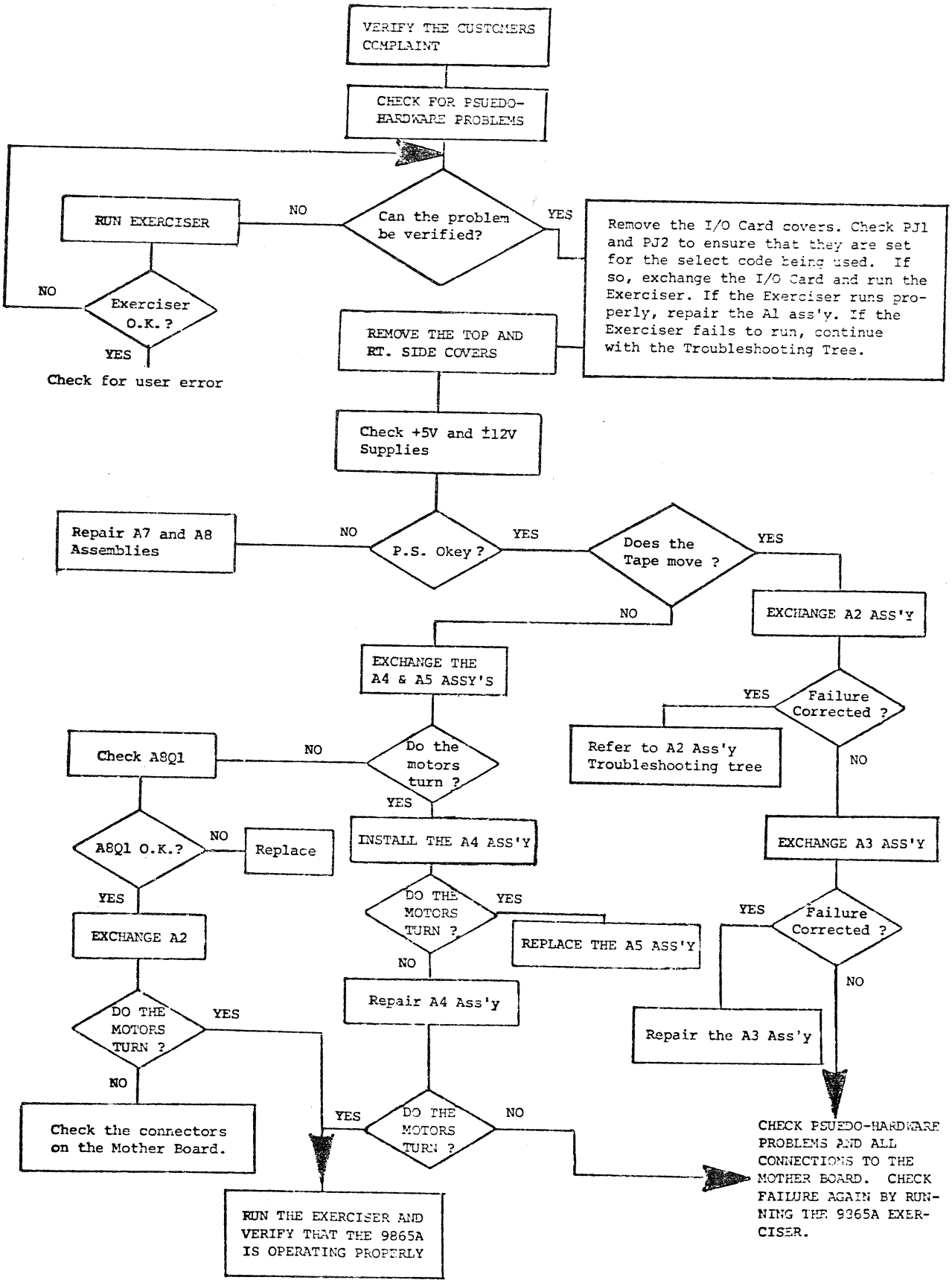


FIGURE 8

THE 9865A CASSETTE MEMORY ASSEMBLIES


VERIFY THE CUSTOMERS COMPLAINT
CHECK FOR PSUEDO-HARDWARE PROBLEMS
RUN EXERCISER
NO
Can the problem be verified?
YES
Remove the I/O Card covers. Check PJ1 and PJ2 to ensure that they are set for the select code being used. If so, exchange the I/O Card and run the Exerciser. If the Exerciser runs properly, repair the A1 ass'y. If the Exerciser fails to run, continue with the Troubleshooting Tree.
NO
Exerciser O.K.?
YES
Check for user error
REMOVE THE TOP AND RT. SIDE COVERS
Check +5V and ±12V Supplies
Repair A7 and A8 Assemblies
NO
P.S. Okey?
YES
Does the Tape move ?
YES
NO
EXCHANGE A2 ASS'Y
EXCHANGE THE A4 & A5 ASSY'S
YES
Failure Corrected ?
Refer to A2 Ass'y Troubleshooting tree
NO
Check A8Q1
NO
Do the motors turn ?
YES
A8Q1 O.K.?
NO
Replace
INSTALL THE A4 ASS'Y
EXCHANGE A3 ASS'Y
YES
EXCHANGE A2
DO THE MOTORS TURN ?
YES
REPLACE THE A5 ASS'Y
NO
YES
Failure Corrected ?
NO
Repair A4 Ass'y
DO THE MOTORS TURN ?
YES
NO
Repair the A3 Ass'y
NO
Check the connectors on the Mother Board.
YES
DO THE MOTORS TURN ?
NO
CHECK PSUEDO-HARDWARE PROBLEMS AND ALL CONNECTIONS TO THE MOTHER BOARD. CHECK FAILURE AGAIN BY RUNNING THE 9865A EXERCISER.
RUN THE EXERCISER AND VERIFY THAT THE 9865A IS OPERATING PROPERLY

EXCHANGING THE (A5) TRANSPORT ASSEMBLY

The transport is on the -hp- Blue Stripe Exchange Program. If you suspect the transport of being defective, it can be exchanged by performing the following procedure:

1.) Switch the Cassette Memory power OFF and unplug the power cord from the power module on the 9865A rear panel.

2.) Remove the 9865A top cover.

3.) Remove the four screws that hold the transport to the mainframe. The screws are located on the top of the transport assembly.

4.) The Transport Assembly includes a PC board that has two blue PC board removers. Lift both blue PC board removers to disconnect the board from the mother board, and lift the transport out of the Cassette Memory.

5.) Reverse steps 1 through 4 to install a new assembly. *

6.) Package the defective Transport Assembly in the special carton provided (-hp- P/N 9211-1779) and return the defective transport for repair.

*Before installing all four screws, ensure that the door OPEN lever operates correctly. It may be necessary to adjust the four screws on the side of the Transport Ass'y to obtain proper alignment of the door and the 9865A front panel.

POWER SUPPLY TEST PROCEDURE (A7 and A8)

1. Switch the cassette memory OFF and remove all assemblies except the A5 (transport), A7, and A8; disconnect the I/O Card from the calculator.

2. Switch the cassette memory ON and measure the power supply voltages. Each supply should be within the tolerances listed below.

+12V	11.8V to 12.2V
-12V	-11.7V to -12.3V
+5V	4.7V to 5.3V

3. If any of the power supplies fail to meet the specification in step 2, repair that supply.

4. Switch the power OFF, reinstall all of the assemblies that were removed in step 1, and switch the power ON.

5. Install the screws that connect the power supply heat sinks to the chassis. The supply can be used for short periods of time with the heat sink disconnected from the chassis, but care should be taken to ensure that the power supply does not become excessively hot as the power supply components may be damaged.

6. Press the REWIND button. While the tape is being rewound, check all of the power supplies to the specifications in step 2.

7. If any supply fails step 6 it must be repaired.

8. If all three supplies have met the requirements in step 6 but the motors still fail to turn, A8Q1 may be defective.

9. If A8U3 was replaced, R15 may have to be padded. To accomplish this:

   a. Remove R15

   b. Measure the +12V supply

   c. Replace R15 with the value indicated on the table below

   d. retest the power supplies beginning with step 1.

Measured Voltage +12 Supply	Selected Value R*15	
	Value	Stock Number
10.64 to 10.71	17.4K	0698-4482
10.72 to 10.79	18.7K	0698-4483
10.80 to 10.87	20.0K	0757-0449
10.88 to 10.95	22.1K	0757-0450
10.96 to 11.03	23.7K	0698-3158
11.04 to 11.11	26.1K	0698-3159
11.12 to 11.19	28.7K	0698-3449
11.20 to 11.27	31.6K	0698-3160
11.28 to 11.35	35.7K	0698-4494
11.36 to 11.43	41.2K	0698-3582
11.44 to 11.51	47.5K	0757-0457
11.52 to 11.59	56.2K	0757-0459
11.60 to 11.67	69.8K	0698-4504
11.68 to 11.75	90.9K	0757-0464
11.76 to 11.83	127 K	0698-4517
11.84 to 11.91	215 K	0698-3454

I/O CARD TEST PROCEDURE (A1)

If exchanging the I/O Card correct the failure, perform the following procedure; use procedure A if the Cassette Memory performs some operations correctly, and procedure B if the Cassette Memory is inoperative or fails following the first operation.

PROCEDURE A

1.) If a MARK TAPE operation is performed, but old data is read instead of the new marks, check (OSØ-OS3) U5.

2.) If a previously marked tape can be read (FIND FILE), but new data cannot be marked on the tape and read; check U6 and U10.

3.) If the Cassette Memory does not detect the clear leader, an open door, or removed protect tabs, check U2.
If operations are aborted as soon as the instructions are given (on the keyboard), check U2 pins 3, 6, and 8 with the tape off of the clear leader, the door closed, and both protect tabs still in the cassette. The U2 outputs should be +5V.

4.) If, when used with a Model 20 Calculator, the interrupt mode is defunct, check U7, U8, U13, and U12b; ensure that PJ3 is not installed.

PROCEDURE B

1.) If a FIND FILE, BACK SPACE, or FORWARD SPACE command is given (using a previously marked tape) and the Cassette Memory cannot find the file or space one file, (i.e., the tape slowly runs to clear leader), check A2 TP2.
If A2 TP2 is high (+5V), check U11, U12a, U9, and U7b.
If A2 TP2 is low (ØV) , check U1, U9, and U8.

2.) If the Cassette Memory does not read previously recorded data or programs correctly, check U3 and U4.

3.) If the Cassette Memory will not perform any operation and the STATUS light is lit, check U2 and Q1 - Q4.

NOTE

Perform each step in procedures A and B. DO NOT SKIP STEPS.

CONTROL LOGIC ASSEMBLY (A2) TEST PROCEDURE

The following procedure will assist you in finding control logic failures. However, the control logic is somewhat sophisticated, and to truely troubleshoot the logic circuits that make the control logic function requires the use of special troulbeshooting techniques and equipment. The following procedure is designed to assist in the repair of most failures, but it will not necessarily point out every failure that may occur. For this reason, the Control Logic Assembly is on the -hp- Red Stripe Program and may be returned to the factory for evaluation.

If, when a keyboard command is given, the 9865A fails to drive the tape, consult the following table:

SYMPTOM	CHECK	PROBABLE CAUSE
Inoperative except for REWIND	300 ns Decoder output	U20, U19, U7
REWIND only inoperative	Rewind FF	U15A, U15B, U16C
No fast tape speed except REWIND	U20	U20
No fast tape speed	U17A	U17A
No reverse operation except REWIND	U20	U20
No reverse operation	U17B	U17B
The motors will not turn	U17 pins 8 or 9 low	U17C
	U2 pin 12 high	'POP' circuit
	U10 pin 8 high	U10C, U19, U7
	U9 pin 8 high	U1B, U9C
	U16 pin 11 high	U1A, U16D
	Check U15B	U15B

CONTROL LOGIC ASSEMBLY (A2) TEST PROCEDURE (cont'd)

If the motors drive the tape, but the A2 ass'y is known to be defective, perform the following tests:

Use a logic probe to check the below test points.

Test Point	In Read Mode Should Normally Be	In Write Mode Should Normally Be
TP1 - 3 KHz Clock	Low	Dim
TP3 - WTC	Low	High
TP4 - FLG	Blinking	Dim
TP6 - 1 of 10 Clock	Dim	Dim
TP9 - WDT	Blinking	Blinking
TP10 - WCL	Low	Dim
TP11 - WMK	Low	Dim

Symptom	Probable Failure
If TP1 is high	3 KHz Write Clock
If TP1 is low	3 KHz Clock, U16B
If TP4 is bad and TP6 Ok	U5A, U8A, U11, U9A, U1
If TP4, TP6, TP10 are bad and TP1 is Ok	U18C, U14, U5A, U8
If TP3 is bad	U16B, U20
If TP6 is bad and TP1 is Ok	U18C, U14, U5A, U8A
If TP10 is bad and TP2, TP6 are Ok	U18D, U11
If TP11 is bad and TP1, TP6 is Ok	U10B
If TP9 is bad	Shift Register or U16A

If all tests are apparently good, but the Cassette Memory does not function properly, the problem may be:

a. Defective Shift Register

b. Defective 3 KHz Clock

c. Defective 1 of 10 bit Decoder

R/W MEMORY BOARD (A3) TEST PROCEDURE

1.) Remove the Cassette Memory top cover.

2.) Switch the Cassette Memory ON.

3.) Measure the voltage on U6 pins 5 and 9. The polarity of the voltages on U6 pins 5 and 9 is dependant upon the conduction states of Q3-Q6. Both voltages must be ± .5V ±10%. If not, Q1 - Q6 has failed. (This test simulates a slow tape speed.)

4.) Switch the 9865A power OFF.

5.) Remove the Transport Ass'y by removing the four screws on the top of the transport and lifting the ass'y out of the Cassette Memory.

CAUTION

IF THE REMAINDER OF THIS PROCEDURE IS PERFORMED WITH THE TRASPORT ASSEMBLY STILL INSTALLED IN THE CASSETTE MEMORY, THE CASSETTE MEMORY WILL BE DAMAGED!

6.) Switch the Cassette Memory power ON.

7.) Temporarily short TP5 to the + (top) side of C19 (+12V)

8.) Measure the voltage on TP6 and pin 5 of U6a.

TP6 = (approx.) +11V

pin 5 = -.95V ±10%

9.) Short TP5 to the - (bottom) side of C20 and check TP6 and pin 5 of U6 as in step number 8. The voltages should be the same, but the polarity of the voltages must be reversed.

10.) Perform steps 7 - 9 by shorting the ±12V supplies to TP 8 and check TP7 and pin 9 of U6b.

11.) Switch the Cassette Memory power OFF, then ON (presets U9a).

12.) Temporarily short TP5 and TP8 to +12V.

13.) TP6 and TP7 must be +11V, if not repeat step 12.

14.) Check TP9 for a logical 1 (+5V). If TP9 is ØV, repeat steps 12 and 13. If TP9 remains low, check U9a.

15.) TP4 should be ØV. If not, U5c or U9b may be defective.

R/W MEMORY BOARD (A3) TEST PROCEDURE (cont'd)

16.) Temporarily short TP8 to the -12V supply. TP7 must be -11V and TP6 +11V. If not repeat steps 12 and 16.

17.) TP4 should be +4 to +5V. If not repeat steps 11 and 16. If TP4 remains low, check U9a, U8, and U3d.

18.) Repeat steps 11, 12, and 14.

19.) Temporarily short TP5 to the -12V supply. TP9 should be ØV . (This checks the .5 US one-shot) If TP9 is not ØV, check U8 and U9.

20.) Switch the power OFF, remove the A2 Ass'y, then switch the power ON.

21.) U1c pin 8 should be +5V; Q7 collector should be +5V; TP2 & TP3 should be +5V.

22.) Switch the power OFF, remove the A3 Ass'y, and use a mini-alligator clip to jumper pins 2 & 4 of U2 to ground (do not worry about pins 1 and 5). Reinstall the A3 Ass'y and switch the power ON.

23.) The voltage on the collector of Q7 should be +5V; the voltage on TP2 and TP3 should be ØV. If not replace U2.

24.) Switch the power OFF and remove the jumpers from step 22. Reinstall the A2 and A3 Ass'ies and switch the power back ON.

25.) TP2, TP3, and the collector of Q7 should be ØV.

26.) When the Cassette Memory has been repaired,return all of the customers assemblies to his 9865A and run the Cassette Memory Exerciser Program.

NOTE

The R/W Memory Board is also on the -hp- Red Stripe Program and may be returned to the factory for evaluation.

MOTOR CONTROL (A4) TEST PROCEDURE

If exchanging the A4 assembly corrects the failure, proceed with the following tests:

1. Switch the cassette memory OFF, remove the A2 assembly, then switch the cassette memory ON.

2. Connect a jumper from ground to A4TP1.

3. Check the following test point voltages:

TEST POINT	VOLTAGE	PROBABLE FAILURE
2	6.0V to 9.0V	CR1, CR2, Q1, Q2
3	6.0V to 9.0V	SHORT ON A4 ASS'Y
4	4.5V to 7.5V	U4
5	6.0V to 9.0V	U2, Q6, Q7
8	6.0V to 9.0V	U2, Q4, Q5

4. Remove the jumper that was installed in step 2.

5. Measure the voltage on TP4. It should be 2.5 to 3.5V. If not U1 or U3 has probably failed.

6. Switch the cassette memory OFF, reinstall the A2 assembly and remove the A3 assembly.

7. Switch the cassette memory ON.

8. Press the key sequence for a SEARCH or FIND FILE operation. The solenoids should energize (click) and the tape should run (slow) forward to the trailing clear leader. (It is not necessary for the motors to turn to perform the following tests).

   Using the 427A, check the following voltages on the defective A4 assembly:

TEST POINT	VOLTAGE	PROBABLE FAILURE
2	3.0 to 6.0V	Q1, Q2
5	3.0 to 6.0V	U2, Q6, Q7
6	11.0 to 13.0V	U2, Q6, Q9
7	0 to .5V	U2, Q4, Q8
8	0 to .5V	U2, Q4, Q5

MOTOR CONTROL (A4) TEST PROCEDURE (cont'd)

9. Press STOP.

10. Press the REWIND button and measure the following voltages with a 427A.

TEST POINT	VOLTAGE	PROBABLE FAILURE
2	9.0 to 13.0V	U1
5	0 to .5V	Q6, Q7, U2
6	0 to .5V	Q6, Q9, U2
7	at least +11V	Q4, Q8, U2
8	at least +9V	Q4, Q5, U2

11. Position the tape on the beginning clear leader. Hold the REWIND button in and measure the voltage on TP2: 3.5 to 4.5V (Checks CR2 and Q3).

When the Motor Control Board has been repaired, return all of the customer's assemblies to his 9865A and run the Cassette Memory Exerciser Program.

MOTHERBOARD CONNECTIONS

TABLE 3

MNEMONIC	A4 ASS'Y P2	A3 ASS'Y P3	A2 ASS'Y P4	A8 ASS'Y P5	A7 ASS'Y P6
+12U				4,D	
CGD				5,E	
LGD	1,A,18,V	1,A,18,V	1,A,24, BB	10,L	
+5V	2,B	2,B	2,B	11,M	
MRV	3,C				
MCM	5,E				
MFR	4,D				
SFR	6,F				
SRV	7,H				
YWDB		4			
ARB		E			
YWDA		3			
ARA		D			
AGD	12,N	6,F		9,K	
YLDR	13		D		
YWPT		5	C		
YWEN		C			
YCIN			3		
+12V	17	17		14,R	
-12V	U	U		15,S	
+17U	8,J			J	
MGD	9,K			7,H	
NRNC	15		12		
NFTC	16	12	13		
NRVC	T		P		
YWTC		13	14		
NPOP		P	R		
YRMK		14	15		
YRDT		R	S		
NRCL		15	16		
YWMK		S	T		
YWDT		16	17		
YWCL		T	U		
+12P				1,A	1,A
+12N				2,B	2,B
+5P				12,N	4,D
+5N				3,C	3,C
-12P				13	5
-12N				P	E
MCT	10,L			8	
MDR	11,M			6,F	
NRWD			N		
YTHA		8			
YTHB		9			

I/O CONNECTIONS

TABLE 3

MNEMONIC	A2 ASS'Y P2	I/O CBLE XA6	I/O ASS'Y XA1
YCNT	11	7	T
YOSØ	22	2	D
YOS1	Z	B	4
YOS2	23	1	A
YOS3	AA	A	1
YODØ	18	6	6
YOD1	V	F	F
YOD2	19	5	E
YOD3	W	E	5
YOD4	20	4	C
YOD5	X	D	3
YOD6	21	3	B
YOD7	Y	C	2
YIDØ	7	11	V
YID1	H	M	18
YID2	8	10	U
YID3	J	L	17
YID4	9	9	N
YID5	K	K	16
YID6	10	8	M
YID7	L	J	12
YFLG	M	H	10
YISØ	5	13	15
YIS1	E	P	K
YIS2	6	12	9
YIS3	F	N	8
LGD		19,W	R,14
CGD		22, Z	
NINT	4	14	11
+5V	-	R	7

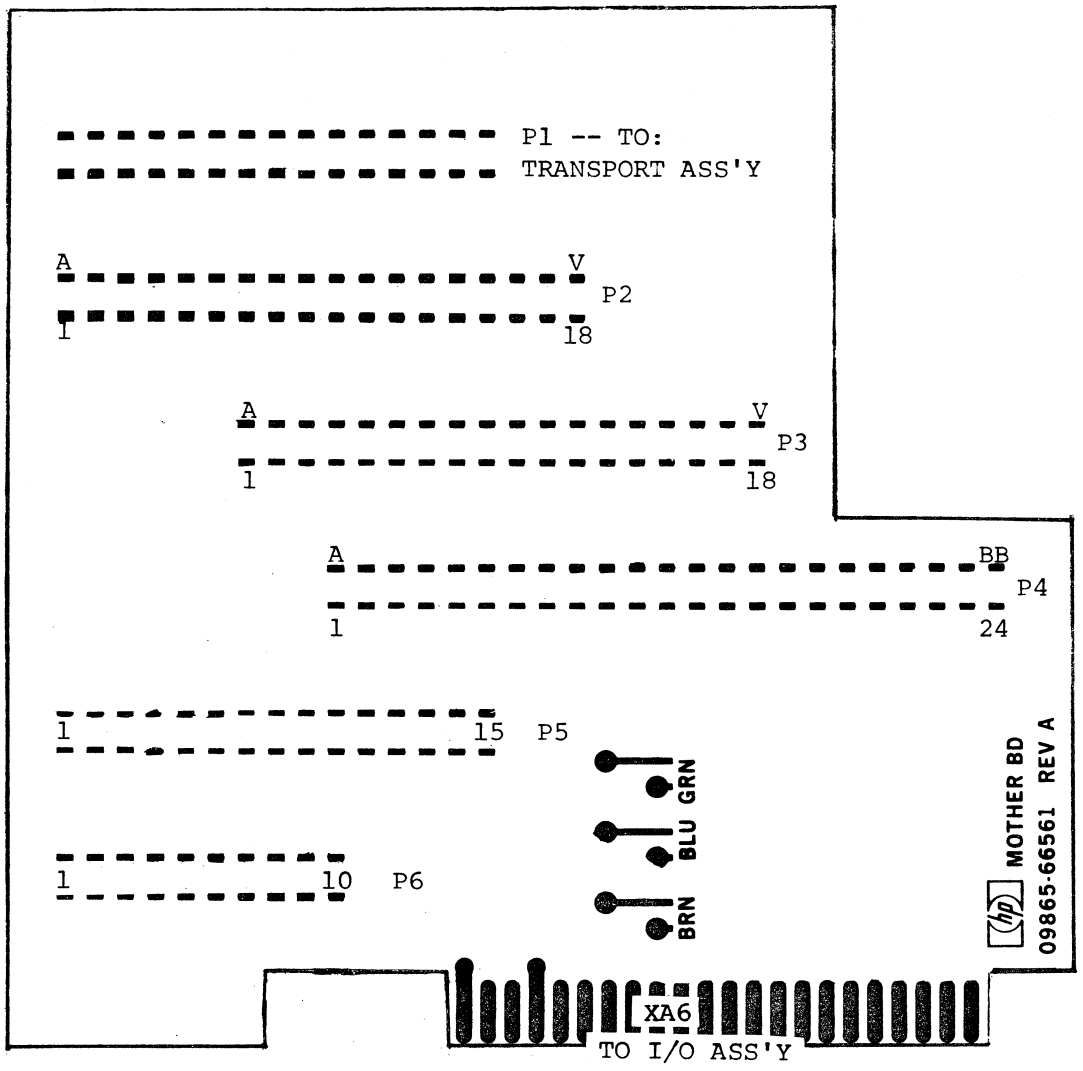
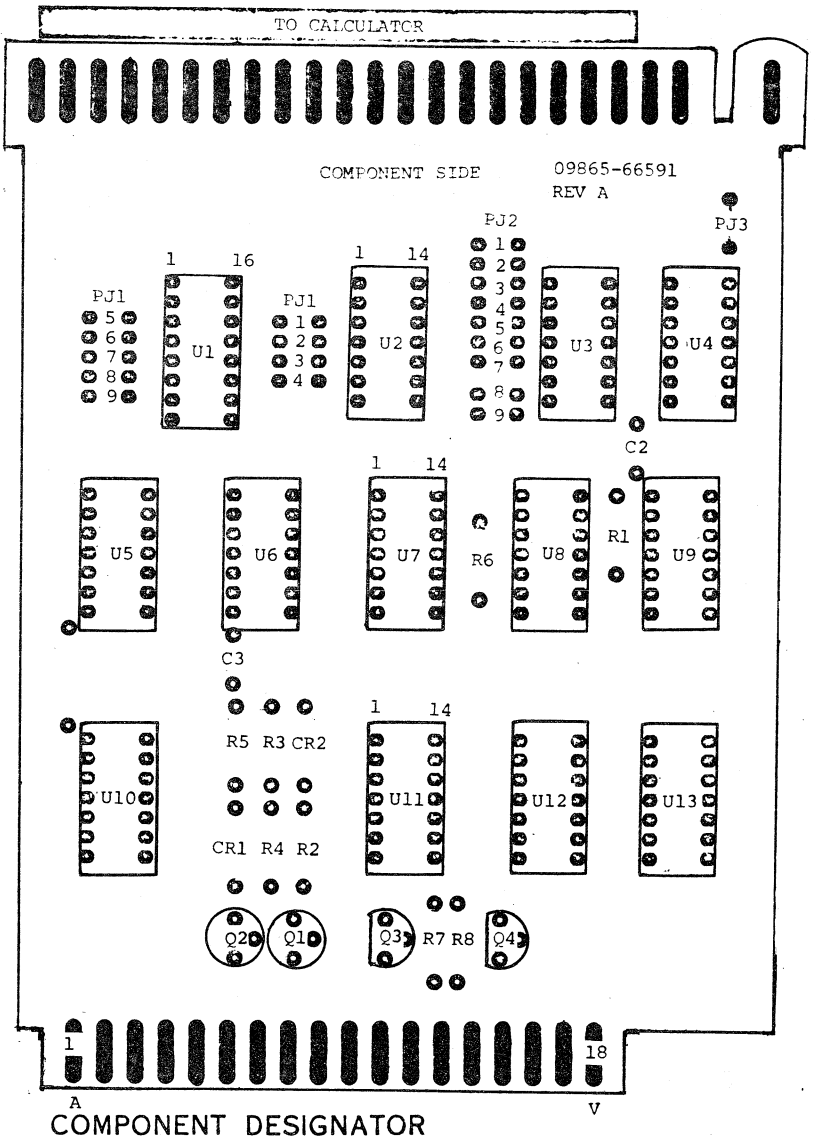


FIGURE 9

A6 MOTHER BOARD PIN CONNECTIONS



COMPONENT DESIGNATOR

COMPONENT DESIGNATOR A1 ASS'Y

I/O CARD

FIGURE 10

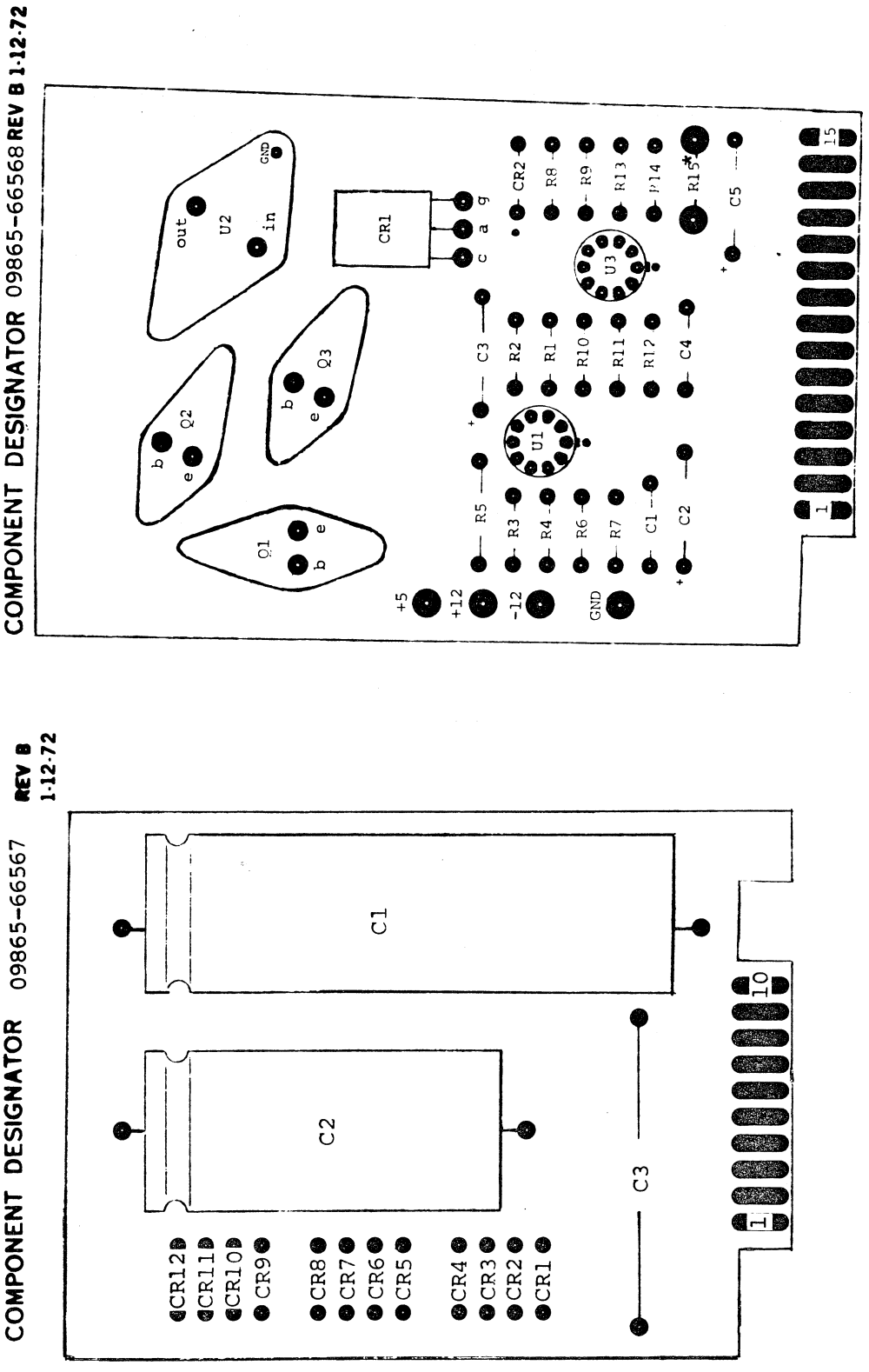


FIGURE 14

COMPONENT DESIGNATORS

POWER SUPPLIES A7 and A8

TABLE 5

9865A PARTS LIST

REFERENCE DESIGNATOR		-hp- PART NO.	TQ	DESCRIPTION		
A1		09865-66591	1	I/O Card		
	C1	0180-0210	1	C: 3.3uf, 15V		
	C2, C3	0150-0093	2	C: .01uf, 100V		
	CR1, CR2	1901-0040	2	Diode: Si, .05A, 30V		
	P1	1251-2188	1	Connector-PC: 2 x 18		
	P2	1251-2048	1	Connector-PC: 2 x 22		
	Q1, Q2	1853-0010	2	XSTR: Si, PNP		
	Q3, Q4	1854-0071	2	XSTR: Si, NPN		
	R1	0684-4721	2	R: fxd, 4.7K 10%		
	R2 thru R8	0684-1021	7	R: fxd, 1K, 10%, 1/4W		
	R9	0684-4721		R: fxd, 4.7K 10%		
	U1	1820-0627	1	IC: U7B93L0159X		
	U2 thru U4	1820-0269	4	IC: SN7403N		
	U5, U6	1820-0598	3	IC: SN74L86		
	U7	1820-0269		IC: SN7403N		
	U8	1820-0511	1	IC: SN7408N		
	U9	1820-0586	2	IC: Dgtl, DM74L04N		
	U10	1820-0598		IC: SN74L86		
	U11	1820-0586		IC: Dgtl, DM74L04N		
	U12	1820-0596	1	IC: Dgtl, DM74L74N		
	U13	1820-0587	1	IC: Dgtl, DM74L10N		
		11200-04101		Cover, I/O Card		
		5040-5948		Cable Boot		
		8120-1746	7'	Cable		
		7120-2939		Label: I/O Cassette		
		09865-61603	1	Cable Ass'y, Input		
		7120-2940		Label: Select Code		
		0362-0249	2	Term: Sleeve		
		0362-0309	2	Sleeve: Cable Term.		
		09862-40040	1	Hood-Connector, LH		
		09862-40050	1	Hood-Connector, RH		
A2		09865-69562	1	Control Logic PC Ass'y		
	C1	0180-0106	1	C: 60uf, 6V		
	C2	0160-3165	2	C: .047uf, 50V		
	C3, C4	0180-0291	2	C: 1uf, 35V		
	C5	0180-1743	1	C: .1uf, 35V		
	C6	0150-0093	6	C: .01uf, 100V		
	C7	0140-0176	1	C: 100pf, 300V		
	C8, C9	0150-0093		C: .01uf, 100V		
	C10	0160-3165		C: .047uf, 50V		
	C11, C12	0150-0093		C: .01uf, 100V		
	C14	0150-0093		C: .01uf, 100V		

REFERENCE DESIGNATOR		-hp- PART NO.	TQ	DESCRIPTION		
A2				(continued)		
	CR1	1901-0040	1	Diode: Si, .05A, 30V		
	CR2	1902-0126	1	Diode: Bkdn,2.61V		
	Q1	1854-0071	1	XSTR: Si, NPN		
	R1	0684-1031	1	R: fxd, 10K, 10%, 1/4W		
	R2	0684-1021	4	R: fxd, 1K, 10%, 1/4W		
	R3	0684-1041	1	R: fxd, 100K, 10%, 1/4W		
	R4	0698-3493	1	R: fxd,4.12K, 10%		
	R5 thru R7	0684-1011	4	R: fxd, 100 ohms, 10%, 1/4W		
	R8	0757-0436	1	R: fxd, MF, 4.32K, 1%		
	R9	0757-0439	1	R: fxd, MF, 6.81K, 1%		
	R10*			Padded Resistor *		
	R11	0684-1021		R: fxd, 1K, 10%, 1/4W		
	R12	0684-1011		R: fxd, 100 ohms, 10%, 1/4W		
	R13, R14	0684-1021		R: fxd, 1K, 10%, 1/4W		
	U1	1820-0537	1	IC: SN7413N		
	U2	1820-0174	2	IC: SN7404N		
	U3, U4	1820-0367	2	IC: SN7495N		
	U5	1820-0077	3	IC: SN7474N		
	U6, U7	1820-0261	3	IC: SN74121N		
	U8	1820-0077		IC: SN7474N		
	U9	1820-0068	1	IC: SN7410N		
	U10	1820-0511	2	IC: SN7408N		
	U11	1820-0174		IC: SN7404N		
	U12	1820-0054		IC: SN7400N		
	U13	1820-0261		IC: SN74121N		
	U14	1820-0055	1	IC: SN7490N		
	U15	1820-0077		IC: SN7474N		
	U16	1820-0511		IC: SN7408N		
	U17	1820-0328	1	IC: SN7402N		
	U18	1820-0054		IC: SN7400N		
	U19	1820-0491	1	IC: SN74145N		
	U20	1820-0701	1	IC: Dgtl		
		4040-0712	1	Extr-PC BD: Red		
		4040-0715	1	Extr-PC BD: Blue		
A3		09865-69563	1	PC BD: R/W Memory		
	C1	0150-0093	10	C: .01uf, 100V		
	C4	0160-0938	2	C: 1000pf, 100V		
	C5	0160-0356	2	C: 18pf, 300V		
	C7	0150-0093		C: .01uf, 100V		
	C8	0160-0170	2	C: .22uf, 25V		
	C10	0160-0938		C: 1000pf, 100V		

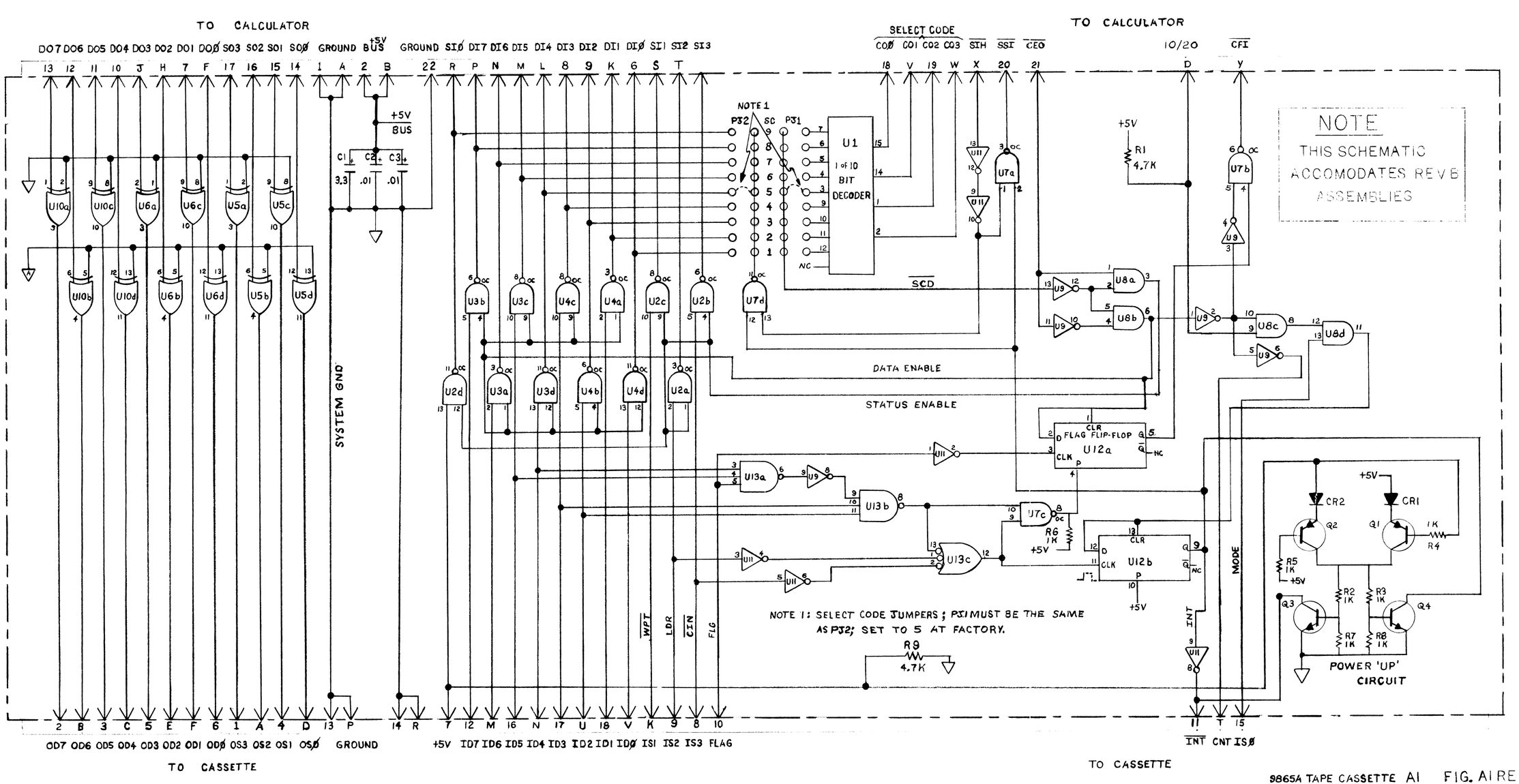
REFERENCE DESIGNATOR	-hp- PART NO.	TQ	DESCRIPTION		
A3			(continued)		
C11	0160-0356		C: 18pf, 300V		
C13	0160-0170		C: .22uf, 25V		
C16	0180-1743	1	C: .1uf, 35V		
C17, C18	0150-0093		C: .01uf, 100V		
C19, C20	0180-0301	2	C: 5uf, 50V		
C21	0140-0176	1	C: 100pf, 300V		
C22 - C27	0150-0093		C: .01uf, 100V		
CR1	1902-3036	1	DIO: BKDN 3.16V		
CR3, CR4 CR9, CR10	1901-0040	4	Diode: Si, .05A, 30V		
Q1	1854-0071	3	XSTR: Si, NPN		
Q2	1853-0020	4	XSTR: Si, PNP		
Q3	1854-0071		XSTR: Si, NPN		
Q4	1853-0020		XSTR: Si, PNP		
Q5	1854-0071		XSTR: Si, NPN		
Q6, Q7	1853-0020		XSTR: Si, PNP		
R1, R36	0684-2221	2	R: fxd, 2.2K, 10%, 1/4W		
R2	0684-2721	1	R: fxd, 2.7K, 10%, 1/4W		
R3	0684-1531	1	R: fxd, 15K, 10%, 1/4W		
R4	0698-3151	2	R: fxd, MF, 2.87K, 1%, 1/8W		
R5	0698-3512	2	R: fxd, MF, 1.18K, 1%, 1/8W		
R6, R7	0698-3179	2	R: fxd, MF, 2.55K, 1%, 1/8W		
R8	0698-3512		R: fxd, MF, 1.18K, 1%, 1/8W		
R9	0698-3151		R: fxd, MF, 2.87K, 1%, 1/8W		
R10	0698-3228	4	R: fxd, MF, 49.9K, 1%, 1/8W		
R11	0757-0442	4	R: fxd, MF, 10K, 1%, 1/8W		
R12	0698-3228		R: fxd, FM, 49.9K, 1%, 1/8W		
R13	0757-0442		R: fxd, MF, 10K, 1%, 1/8W		
R14	0684-1031	4	R: fxd, 10K, 10%, 1/4W		
R15	0684-4701	2	R: fxd, 47 ohms, 10%, 1/4W		
R19	0684-3321	2	R: fxd, 3.3K, 10%, 1/4W		
R20	0684-1031		R: fxd, 10K, 10%, 1/4W		
R21	0684-2231	2	R: fxd, 22K, 10%, 1/4W		
R22	0698-3228		R: fxd, MF, 49.9K, 1%, 1/8W		
R23	0757-0442		R: fxd, MF, 10K, 1%, 1/8W		
R27	0684-4701		R: fxd, 47 ohms, 10%, 1/4W		
R28	0684-1031		R: fxd, 10K, 10%, 1/4W		
R29	0684-3321		R: fxd, 3.3K, 10%, 1/4W		
R30	0698-3228		R: fxd, MF, 49.9K, 1%, 1/8W		
R31	0757-0442		R: fxd, MF, 10K, 1%, 1/8W		
R32	0684-1031		R: fxd, 10K, 10%, 1/4W		
R33	0684-2231		R: fxd, 22K, 10%, 1/4W		
R34	0683-3915	1	R: fxd 390 ohm 5%		
R37	0684-6821	1	R: fxd, 6.8K, 10%, 1/4W		
R35	0683-2015	1	R: fxd 200 ohm 5%		
U1	1820-0511	1	IC: SN7408N		
U2	1820-0068	1	IC: SN7410N		
U3	1820-0054	1	IC: SN7400N		

REFERENCE DESIGNATOR		hp PART NO.	TQ	DESCRIPTION		
A3				(continued)		
	U4	1820-0174	1	IC: SN7404N		
	U5	1820-0328	1	IC: SN7402N		
	U6	1826-0019	1	IC: Op amp		
	U8	1820-0261	1	IC: 74121N		
	U9	1820-0077	1	IC: SN7474N		
		4040-0713	1	Extr- PC BD: Orange		
		4040-0715	1	Extr- PC BD: Blue		
A4		09865-66564	1	Motor Control Assembly		
	C1	0160-0160	1	C: .008uf, 200V		
	C2	0150-0121	2	C: .1uf, 50V		
	C3, C4	0150-0093	2	C: .01uf, 100V		
	C5	0150-0121		C: .1uf, 50V		
	Q1	1853-0010	1	XSTR: Si, PNP		
	Q2	1854-0039	1	XSTR: Si, NPN		
	Q3, Q4,	1853-0027	3	XSTR: Si, PNP		
	Q5	1854-0556	4	XSTR: Si, NPN		
	Q6	1853-0027		XSTR: Si, PNP		
	Q7, Q8, Q9	1854-0556		XSTR: Si, NPN		
	R1	0698-0083	1	R: fxd, MF, 1.96K, 1%		
	R2	0698-3279	1	R: fxd, MF, 4.99K, 1%		
	R3	0757-0442	1	R: fxd, MF, 10K, 1%		
	R4	0684-5611	1	R: fxd, 560 ohms, 10%		
	R5	0684-2231	1	R: fxd, .22K, 10%		
	R6	0687-1521	1	R: fxd, 1.5K, 10%		
	R7	0684-2211	1	R: fxd, 220 ohms, 10%		
	R8	0757-0472	1	R: fxd, MF, 200K, 1%		
	R9	0811-3143	1	R: fxd, 10 ohms 1%		
	R10	0698-7313	1	R: fxd, MF, 19.8K, .1%		
	R11	0698-7398	1	R: fxd, MF, 6.124K, .1%		
	R12	0698-7861	1	R: fxd, MF, 25.42K, .1%		
	R13	0698-7681	1	R: fxd, MF, 15.33K, .1%		
	R14	0698-6378	1	R: fxd, MF, 14.9K, .1%		
	R15	0698-4473	1	R: fxd, MF, 8.06K, 1%		
	R16, R17	0684-8211	2	R: fxd, 820 ohms, 10%		
	R18	0687-6801	4	R: fxd, 68 ohms, 10%		
	R19	0684-1021	2	R: fxd, 1K, 10%		
	R20, R21	0687-6801		R: fxd, 68 ohms, 10%		
	R22	0684-1021		R: fxd, 1K, 10%		
	R23	0687-6801		R: fxd, 68 ohms, 10%		

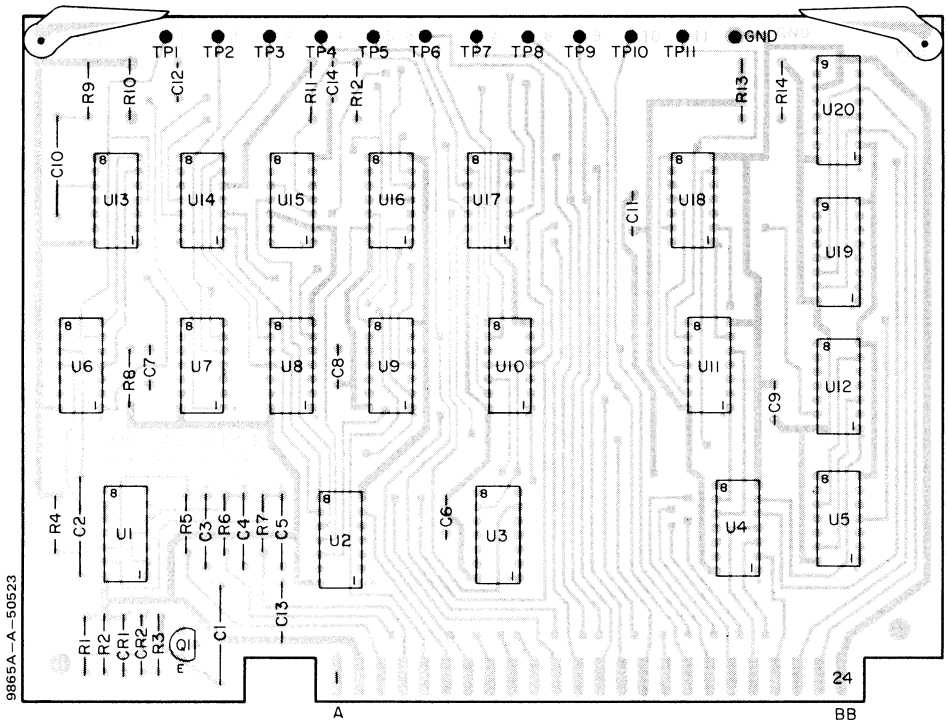
REFERENCE DESIGNATOR		-hp- PART NO.	TQ	DESCRIPTION		
A4				(continued)		
	U1	1820-0471	1	IC: SN7406N		
	U2	1820-0094	1	IC: DGTL, Quad 2		
	U3, U4	1820-0203	2	IC: Opr Ampl		
	CR1	1902-0048	1	Diode: Bkdn, 6.81V		
	CR2	1901-0040	1	Diode: Si, .05A, 30V		
	CR3	1902-0041	1	Diode: Bkdn, 5.11V		
	L1	9140-0018	1	Coil: RF Choke, 1uH		
		4040-0714	1	Extr-PC BD: Yellow		
		4040-0715		Extr-PC BD: Blue		
A7		09865-66567	1	Power Supply Filter Board		
	C1	0180-2487	1	C: 2100uf, 30V		
	C2	0180-2101	1	C: 4000uf, 15V		
	C3	0180-1802	1	C: 150uf, 40V		
	CR1 thru CR12	1901-0045	12	Diode: Si, .75A, 100V		
		4040-0754	1	Extr-PC BD: Blue		
		4040-0755	1	Extr-PC BD: Violet		
A8		09865-66568	1	Power Supply Regulator Assembly		
	C1	0160-3456	2	C: 1000pf		
	C2, C5	0180-1746	2	C: 15uf, 20V		
	C3	0180-0229	1	C: 33uf, 10V		
	C4	0160-3456	1	C: 1000 PF		
	Q1 - Q3	1854-0072	3	XSTR: 2N3054		
	R1, R2	0757-0273	2	R: fxd, MF, 3.01K, 1%		
	R3	0684-1011	2	R: fxd, 100 ohms, 10%		
	R4	0684-1021	2	R: fxd, 1K, 10%		
	R5	0811-2546	1	R: fxd, .56 ohms, 5%		
	R6	0698-3153	1	R: fxd, MF, 3.83K, 1%		
	R7	0698-3268	1	R: fxd, MF, 11.5K, 1%		
	R8	0684-6801	1	R: fxd, 68 ohms, 10%		
	R9	0757-0283	1	R: fxd, MF, 2K, 1%		
	R10	0684-1011		R: fxd, 100 ohms, 10%		
	R11	0684-1021		R: fxd, 1K, 10%		

REFERENCE DESIGNATOR		-hp- PART NO.	TQ	DESCRIPTION		
A8				(continued)		
	R12	0698-8062	1	R: fxd, 4.7 ohms, 10%		
	R13	0698-4440	1	R: fxd, MF, 3.4K, 1%		
	R14	0698-3515	1	R: fxd, MF, 5.9K, 1%		
	R15	See Test Procedure		Padded Value		
	U1	1820-0196	2	IC: U5R7723393		
	U2	1820-0430	1	IC: Linear		
	U3	1820-0196		IC: U5R7723393		
	CR1	1884-0068	1	Thyristor		
	CR2	1902-0049	1	Diode: Bkdn, 6.19V		
		09865-01168	1	Bracket, Heat Sink		
		4040-0715	1	Extr-PC BD: Blue		
		4040-0716	1	Extr-PC BD: Gray		
A6		09865-26561	1	Mother Board		
	P1	1251-2035	2	Connector, PC (2 x 15)		
	P2, P3	1251-2026	2	Connector, PC (2 x 18)		
	P4	1251-2582	1	Connector, PC (2 x 24)		
	P5	1251-2035		Connector, PC (2 x 15)		
	P6	1251-2034	1	Connector, PC (2 x 10)		
A5		09865-69902	1	Transport Assembly		
CHASSIS MOUNTED						
	S1	3101-0014	1	Switch: P.B., Rewind		
	S2	3101-1244	1	Switch: P.B., Power		
	T1	9100-3266	1	Power Transformer		
	L1, L2	9140-0029	2	Coil		
		5060-9422	1	Line Module		
		2110-0201	1	Fuse: .25 amp, 240V		
		2110-0202	1	Fuse: .50 amp, 120V		
		8120-1379	1	AC Power Cord		
		7124-2308		Label: 240V/120V		
		7120-2965		Label: Select Code 5		

REFERENCE DESIGNATOR	-hp- PART NO.	TQ	DESCRIPTION
			(continued)
	7120-2940		Label: Select Code 1-9
	5060-8577		Top Cover Assembly
	5060-0703		Frame Assembly
	5040-7004		Receptacle, Buffer
	5040-0700		Hinge
	5040-7003		Cassette Door Assembly
	5000-8587		Bottom Cover
	8500-0810		Tape Head Cleaner
	8520-0023		Head Cleaning Swabs
	9162-0050		Tape Cassette
	7120-1254		Identification Plate
	9220-1545		Foam Pad
	09865-90000		Peripheral Manual
	09865-90001		Storage Forms
	09865-90003		Service Manual
	09810-90020		Operating Manual
	11269A		9865A Service Kit
The 11269A	Service Kit includes:		
	11265-69521		Cassette Memory Control Block
	09865-69902		Transport Ass'y
	09865-69562		Control Logic Ass'y
	09865-69563		Read/Write Memory Ass'y
	09865-66591		Interface Card
	09865-66564		Motor Control Ass'y
	09865-66567		P.S. Filter Ass'y
	09865-66568		P.S. Regulator Ass'y
	2110- 0201	3	Fuse; .25A
	2110- 0202	3	Fuse; .50A
	8500-0810		Magnetic Head Cleaner
	9162-0050	2	Tape Cassette
	8520-0023	100	Applicators, Head Cleaning
	09810-90035	1	Cassette Memory Exerciser Card
	5060-0091		10 pin Extender
	09865-66515		15 pin Extender
	09865-66514		24 pin Extender
	5060-5985		18 pin Extender
	09865-90003		Service Manual
			Miscellaneous Packaging



98654A TAPE CASSETTE AI FIG. AI REV B
I/O BOARD 09865-66591



COMPONENT SIDE

A62

-hp- Part No. 09865–66562 Rev B

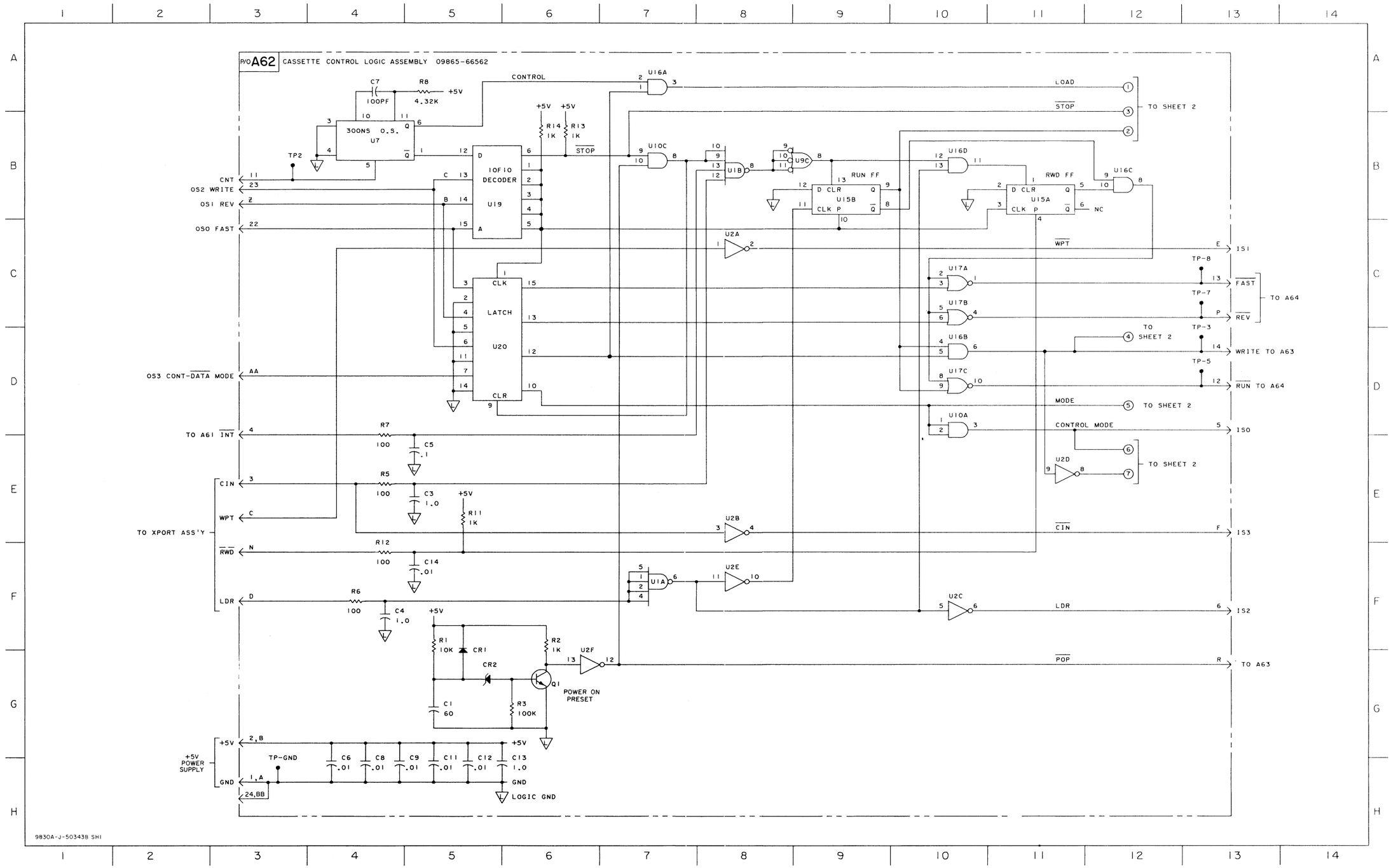
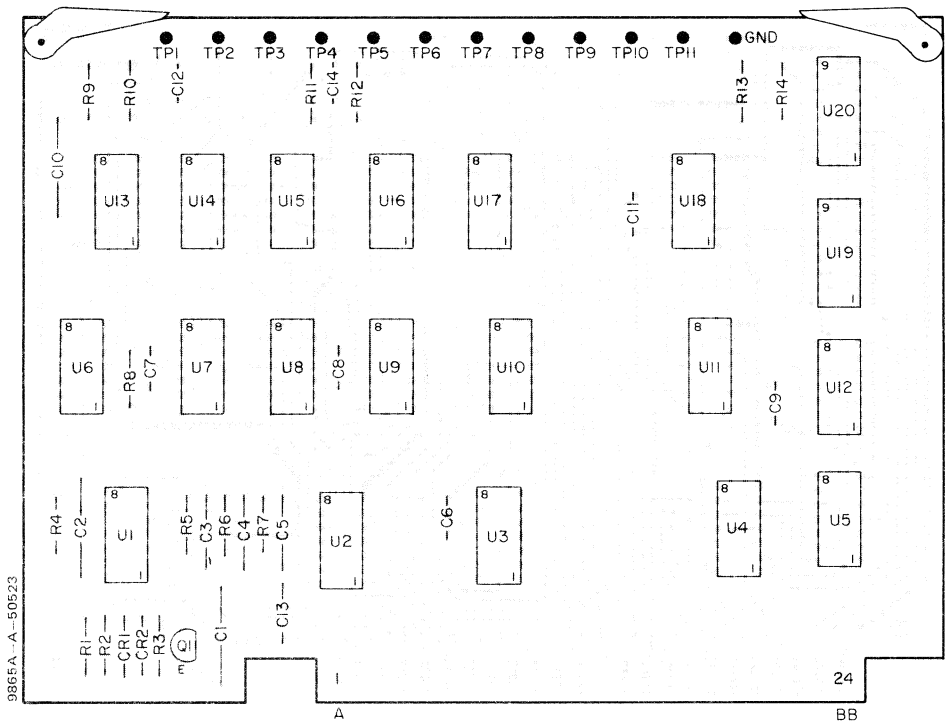


Figure A2 Control Logic Assembly A62 (Sheet 1 of 2)



COMPONENT SIDE

A62

-hp- Part No. 09865–66562 Rev B

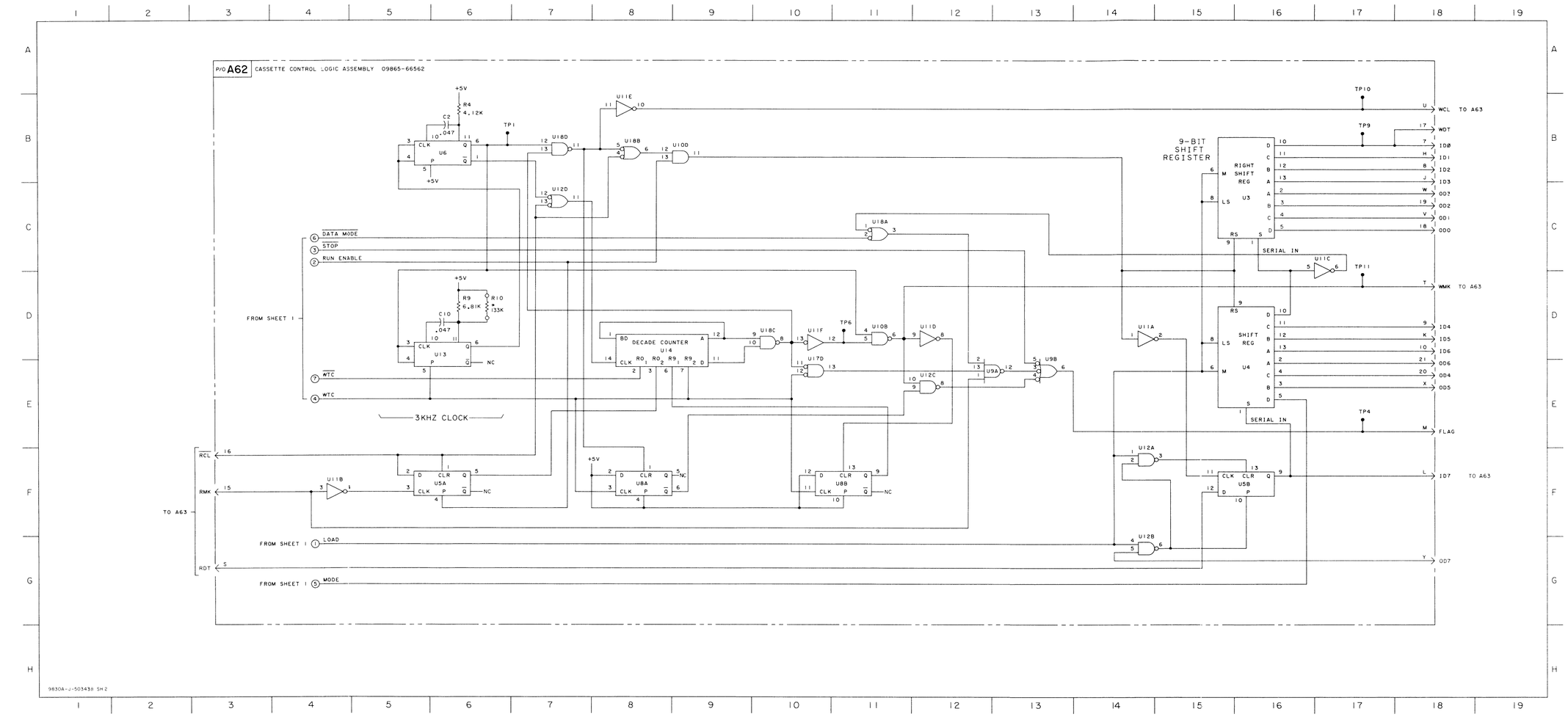
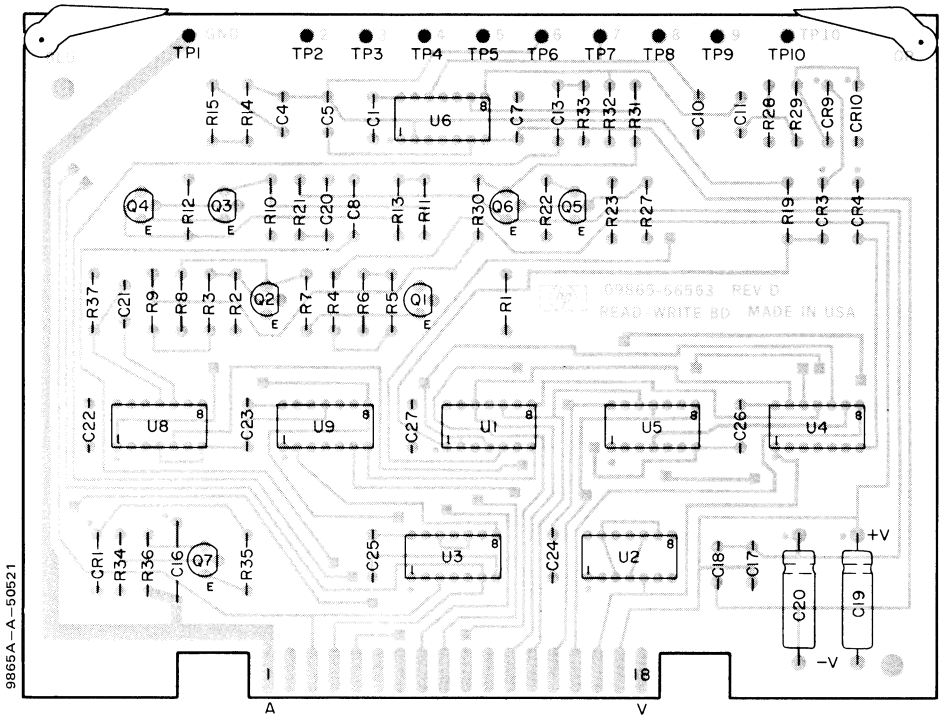


Figure A2 Control Logic Assembly A62 (Sheet 2 of 2)



COMPONENT SIDE

A63

-hp- Part No. 09865–66563 Rev D

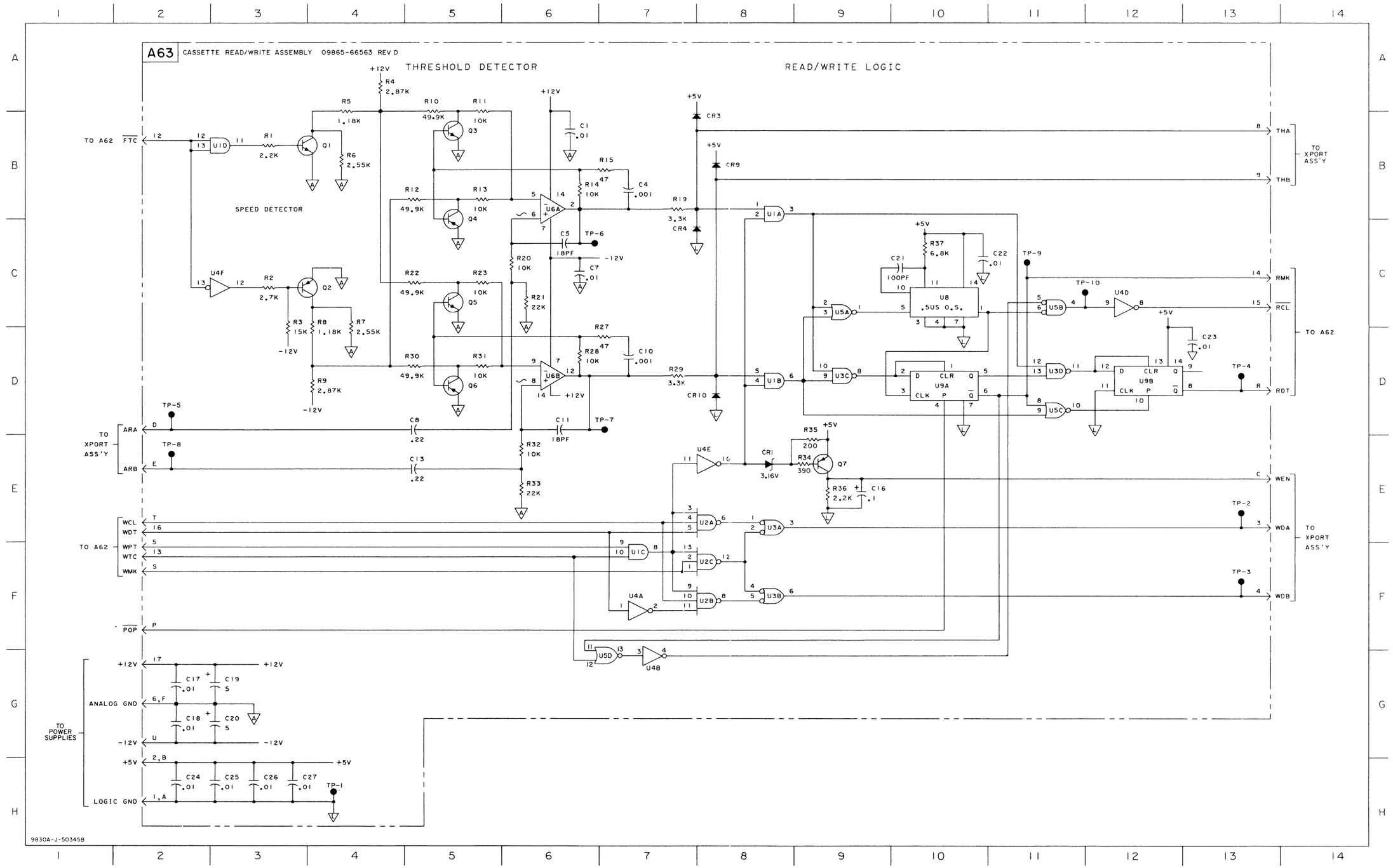
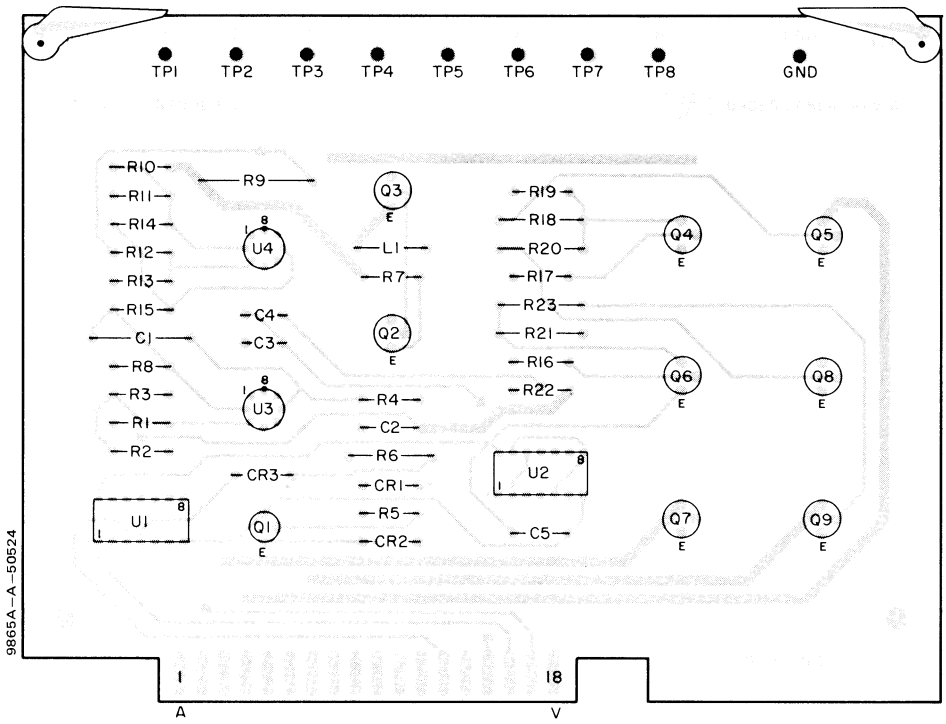


Figure A3 Cassette R/W Memory Assembly A63



COMPONENT SIDE

A64

-hp- Part No. 09865–66564 Rev B

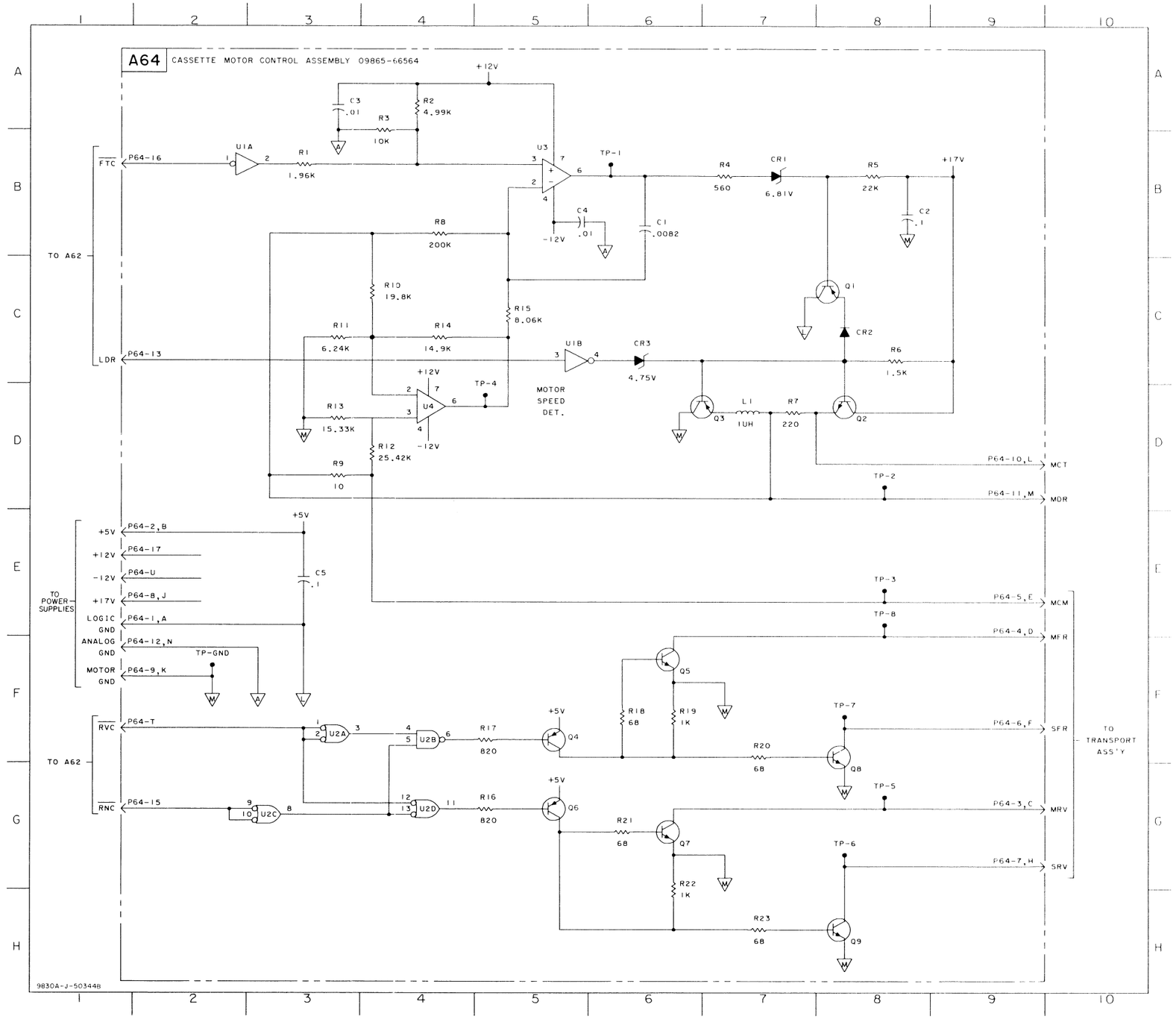


Figure A4 Motor Control Assembly A64

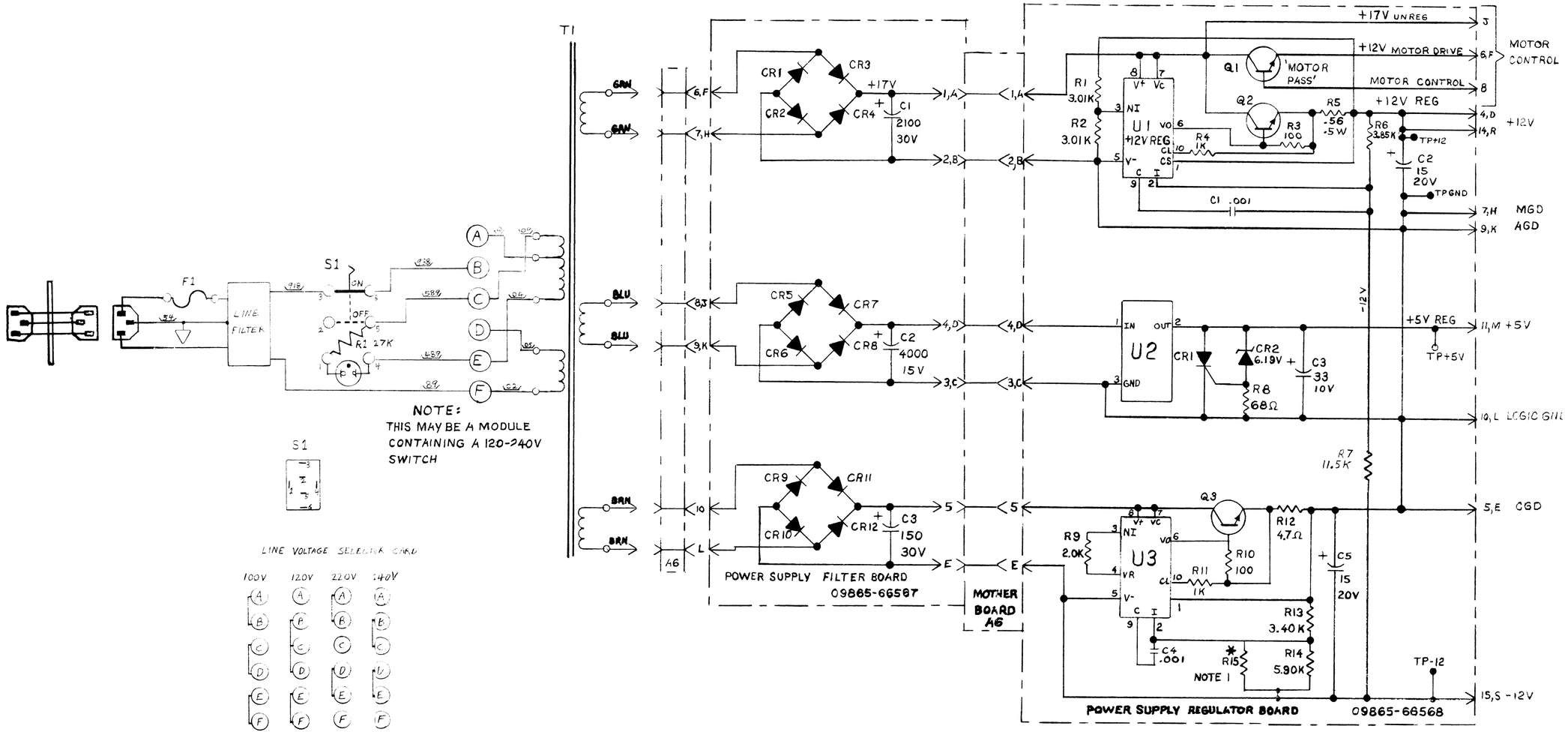


FIG. A7
POWER SUPPLIES

PART NO. 09865–90003

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